

PCILite.com

The Easy-to-use PCI Bus Interface

PCILite Datasheet

Version 3.1
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Website: www.pcilite.com
Email: info@pcilite.com
Phone: +27 11 315-8316
Fax: +27 11 315-1711

A product developed by

The logo for ASIC Design Services features the word "ASIC" in a large, bold, serif font. A small red triangle is positioned above the letter "I". Below "ASIC" is the phrase "Design Services" in a smaller, italicized serif font. A thin horizontal line is placed between "ASIC" and "Design Services".

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VERSION INFORMATION

The differences between version 3.1 and 3.0 are given here.

<u>PAGE</u>	<u>CHANGE MADE</u>
36	Changed pin 7 to TMS
38	Changed pinout for 16-bit 144 TQFP.
40	Changed pinout for 32-bit 144 TQFP.
42	Changed pin 11 to TMS

PREFACE

This document offers a full technical description of PCILite. PCILite complies with the PCI Local Bus Specification; Revision 2.2 and parts of this specification are included herein. This document however does not include the full PCI Local Bus Specification, Revision 2.2. If the user requires any further information about the PCI Local Bus Specification, Revision 2.2 it can be found at:

- PCI Special Interest Group
<http://www.pcisig.com>

FEATURES

PCI is a synchronous bus architecture with all data transfers being performed relative to a bus clock. A PCI TARGET device responds to the transfer based on its address and transfer command. A PCI MASTER device initiates transfers on the bus. The system MASTER sets up each card's address, and enables the device.

Most applications require only a TARGET PCI Device. PCILite was born out of the requirement for a simple PCI interface. PCILite is simply a TARGET. PCILite can accept transfers from any MASTER with DMA.

PCILite has an INTEL like microprocessor backend interface. Simple read, write and chip-select signals are provided. The duration of these signals is software programmable. A user address and data bus connects peripherals.

There are additional user definable pins. These pins can act as either inputs or outputs or can be programmed to be chip-selects.

PCILite is available in an 8-bit, 16-bit and a 32-bit version. The only difference between the different versions, apart from the data-bus width and number of user lines is the package details.

Intended Use

32-Bit, 33MHz, 5V or 3.3V PCI applications

Simple Backend for Asynchronous RAM, I/O Subsystems

Conversion of old ISA designs to PCI.

Key Features

Standard PCI/TARGET Registers

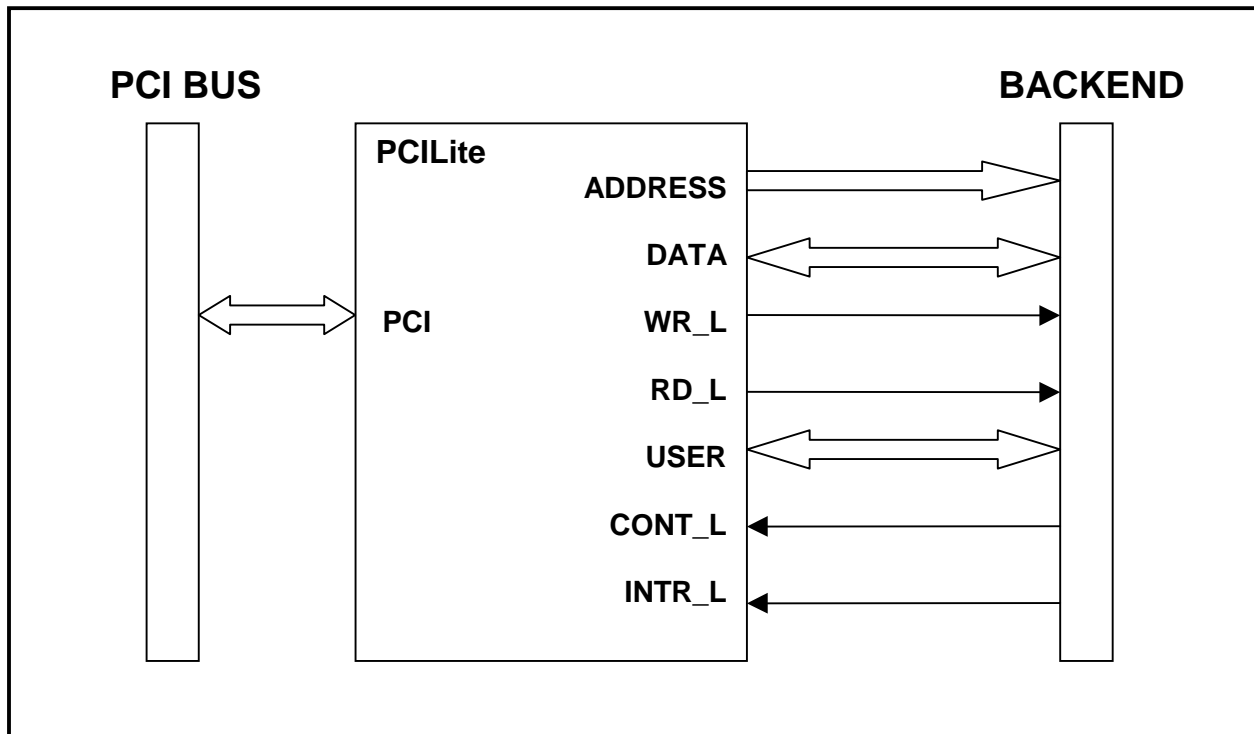
Interrupt Capability

Flexible Backend Data Flow Control

User Definable IO - Select between an input/output or chip select

Compliant with the PCI 2.2 Specification

528 Mbits/s peak transfer rate



1. GENERAL DESCRIPTION

1.1 PCI BACKGROUND

The PCI Local bus is one of the most successful standards in history, serving as the main general-purpose bus in virtually every desktop computer throughout the world. A great deal of this success can be attributed to PCI's original forward thinking design.

PCI is a synchronous bus architecture with all data transfers being performed relative to a bus clock. The initial PCI specification permitted a maximum clock rate of 33Mhz allowing one bus transfer to be performed every 30 nanoseconds. Later, Revision 2.1 of the PCI specification extended the bus definition to support operation at 66Mhz, but the vast majority of today's computers continue to implement a PCI bus that runs at a maximum speed of 33Mhz. The design of the 66Mhz system is exactly the same as that for 33MHz.

There are basically three types of PCI interface devices used on the PCI bus: MASTER, TARGET and BRIDGE. MASTER devices initiate transfers on the bus. A TARGET device responds to the transfer based on its address and transfer command. After power up, all PCI devices are disabled. The system MASTER sets up each card's address, and enables the device. The system MASTER has an additional function of arbitrating between MASTERS. The host processor talks through the system MASTER. A combination of a MASTER plus TARGET on the same device is possible. Most applications require only a TARGET. The host processor talks to the card via the system MASTER.

The PCI BRIDGE is the third PCI device. A PCI BRIDGE expands a PCI bus. Because of strict signal loading constraints, the PCI bus normally does not have more than 5 slots. The PCI BRIDGE expands the PCI bus into more sub-busses.

The PCI standard specifies a standard block of registers. All PCI devices have these registers. Software drivers for the PCI card must access these registers via BIOS calls. Once the value of the BASE address register has been read, processor transfers to the card can be made. The developer must have access to the PCI BIOS specification. No additional tools, other than the standard software development tools, are needed to write drivers for a PCI card. This task can be simplified through the use of driver generation software.

For the designer, PCI has complicated the design of standard system cards. A wide range of PCI - interface devices are available to today's designer, but these devices tend to be rather complex in nature. This is because they are aimed at the top-end performance applications that the PCI bus can offer.

One of the biggest problems designing on PCI is the learning curve a designer has to work through. The manuals on these standard devices can be several hundred pages thick. Most of the circuitry contained inside these devices are not part of the PCI specification, and make the learning curve an even more daunting task. Standard interface devices also usually require additional external circuitry (such as configuration PROM and CPLD).

PCILite was born out of the requirement for a simple interface. PCILite is simply a PCI TARGET. It can accept DMA transfers from any MASTER with DMA. This simple solution allows old ISA card designs to be converted to PCI, requiring minimum effort from the designer.

PCILite has an INTEL like microprocessor back - end interface. Simple read, write and chip-select signals are provided. The duration of these signals is software programmable. A user address and data bus connects peripherals. There are additional user definable pins. These pins can act as either inputs or outputs or can be programmed to be chip-selects.

PCILite is currently available in an 8-bit, 16-bit or 32-bit version, however, because PCILite is implemented

on an Actel FPGA, it is possible for ASIC Design Services to modify the design if the user so requires. In this way, it is possible for ASIC Design Services to provide an application specific PCI interface for the user.

Because of the simplicity of PCILite, a PCI application can be developed in a very short space of time.

1.2 MAJOR FEATURES

1.2.1 PCI BUS CYCLES

The Burst Transaction

The basic mechanism of data transfer in PCI is the burst transaction.

A master initiates a transfer. An address is placed on the PCI Address/data bus. A command is placed on the PCI CBE bus. The command tells the targets what type of transfer it wants to do. Typical instructions are Memory read/writes and IO read/writes. The master then drives the FRAME_L signal low, indicating the beginning of the transfer.

A target compares this address to its BASE pointer, and if a hit is found, it drives the DEVSEL_L signal low.

Configuration Cycles

After power up all PCI cards in a system are disabled. The PCI BIOS uses configuration registers to setup each card on the bus.

Configuration, read and write cycles are used to define and determine the status of the target's configuration registers. Configuration cycles are the only type of transactions that use the IDSEL signal; a unique signal in each slot that allows the slot to be selected for configuration cycles. Register selection is defined by the contents of the address (bits 7 down to 2). PCILite supports burst transactions to configuration space if required.

Once the base pointers have been set up, the device is enabled to respond to PCI transfers. Configuration cycles always take two clock cycles per transfer. PCILite also maps the configuration registers to memory. This allows the user to bypass the PCI BIOS.

1.2.2 REGISTERS

PCI Configuration Registers

A standard block of registers, common to all PCI devices is implemented in PCILite. These registers describe the PCI device to the bus. For example, they specify if the device is IO or memory mapped, and where the device is mapped. It also contains registers for interrupts. A feature of PCILite is that all PCI configuration registers are also memory mapped, allowing the user to directly manipulate the card's setup, and thus not having to go through the system's PCI bios.

Internal Registers

There are a few registers internal to PCILite that are PCILite specific. These registers define the read and write cycle timing, and define the function of each user pin. The HOLD mode is also activated using an internal register.

1.2.3 BACKEND INTERFACE

The backend consist of an address and bi-directional data bus. Active-low asynchronous read (RD_L) and write (WR_L) signals are provided. The setup and hold time of the data, address and chip-select lines can be programmed using internal registers SU and HLD. The width of the RD_L and WR_L signals is also programmable using the DU registers. Chip selects are available using the user pins. This decodes user address bits A[13:9] in the 32-bit PQ208 and 16-bit versions, A[13:10] in the 32-bit TQ144 version and A[13:11] in the 8-bit version and gives an active low chip-select on the user pins when activated. There is a global chip-select available on user pin 20 (user pin 13 or 5 in the 32-bit TQ144 and 8-bit versions respectively) that goes active (low) during accesses mapped to the backend.

A special cycle mode called the HOLD mode can be enabled. When enabled, the user must also select the HOLD TYPE that will be used. When the HOLD TYPE is set as EDGE, the transfers are started, but during the time that RD_L or WR_L is active, PCILite waits for a falling edge on signal CONT_L, before continuing with the cycle. When the HOLD TYPE is set as LEVEL, the transfers are started, but during the time that RD_L or WR_L is active, PCILite waits for signal CONT_L to be high, before continuing with the cycle. So if CONT_L is always high, PCILite will not wait before continuing the cycle. HOLD mode is handy when interfacing with devices, that might not be ready when the PCI bus wants to make transfers.

User Pins

32-Bit PQ208

There are 25 user pins USR[24:0]. Each pin can be individually programmed to be an INPUT, OUTPUT or chip-select. On power up the pins are defined as inputs. User pin USR[20] can serve as a global active low chip-select during accesses mapped to the backend, or enabled as a user IO.

32-Bit TQ144

There are 14 user pins USR[13:0]. Each pin can be individually programmed to be an INPUT, OUTPUT or chip-select. On power up the pins are defined as inputs. User pin USR[13] can serve as a global active low chip-select during accesses mapped to the backend, or enabled as a user IO.

16-Bit

There are 25 user pins USR[24:0]. Each pin can be individually programmed to be an INPUT, OUTPUT or chip-select. On power up the pins are defined as inputs. User pin USR[20] can serve as a global active low chip-select during accesses mapped to the backend, or enabled as a user IO.

8-Bit

There are 6 user pins USR[5:0]. Each pin can be individually programmed to be an INPUT, OUTPUT or chip-select. On power up the pins are defined as inputs. User pin USR[5] can serve as a global active low chip-select during accesses mapped to the backend, or enabled as a user IO.

Interrupts

There is an edge triggered interrupt pin. A falling edge on this pin will cause INTAN to go low (If interrupts are enabled on PCILite). Interrupts are cleared using the dedicated PCI register contained within PCILite. An interrupt can also be forced by writing a one to the FORCE_INT register.

2. PIN DESCRIPTION

Pin Name	User/PCI	Pin Type	Description
A[13:0]	USER	OUTPUT	User Address lines. These lines are Double word addresses, and are valid when a RD_L or WR_L occurs. This address will be the same as the PCI address [15:2]. In burst transactions it is auto incremented.
AD[31:0]	PCI	Bi-directional	PCI Multiplexed 32-bit address and data bus. A valid address is indicated by FRAME _n being asserted
CBE[3:0]	PCI	INPUT	Bus command and byte enable information. During the address phase, the lower 4 bits define the bus command. During the data phase, they define the byte enables. PCILite ignores the byte enables, and all transfers are presumed to be Double word.
CLK	PCI	INPUT	33Mhz clock INPUT to PCILite
D[31:0] or D[15:0] or D[7:0]	User	Bi-directional	This is the data bus to the user's circuitry.
DEVSEL _n	PCI	OUTPUT (STS)	Active low OUTPUT from PCILite indicating that it is the Target of the current access.
FRAME _n	PCI	INPUT	Active low signal indicating the beginning and duration of an access. While FRAME _n is asserted, data transfers continue.
GND	PCI/USER	Power	Power/signal ground
IDSEL	PCI	INPUT	Active High Target select used during configuration read and write transactions.
INTAN	PCI	Open Drain	Active-low interrupt request.
INTR_L	USER	INPUT	Edge-triggered interrupt pin. A falling edge on this pin will cause INTAN to go low (If interrupts are enabled on PCILite). Interrupts are cleared using the dedicated PCI register contained within PCILite.
IRDYN	PCI	INPUT	Initiator ready pin. Active LOW signal indicating that the bus MASTER is ready to complete the current data phase transaction.
NC	USER	Not connected	
PAR	PCI	Bi-directional	Parity signal. Parity is even across AD[31:0] and CBE[3:0]
PERR _n	PCI	Tri-statable OUTPUT	Active low parity error signal.
RD_L	USER	OUTPUT	User active low read pin. When low, a read operation is performed on the user's circuitry. Data must be valid on the rising edge of this signal. The duration of this signal is programmable, to be 30ns, 60ns, 90ns, 120ns, 150ns, 180ns, 210ns etc. up to 480ns, or can be lengthened by the use of the CONT_L signal. The user should note that the uses of very slow transfers, violates the PCI specification. This violation of the PCI spec should not cause problems, because PCI bridges allows for much longer delays in transactions.
RST _n	PCI	INPUT	Active LOW asynchronous reset.
STOP _n	PCI	Tri-statable OUTPUT	Active LOW signal from PCILite requesting termination of the current transaction. If CONT_L causes the read or write transaction to be too long, then this signal will be used to terminate the transfer. The masters will then terminate the transfer, and re-try the transfer.
SERR _n	PCI	Open Drain	Active low system error. This signal reports PCI address parity errors.

Pin Name	User/PCI	Pin Type	Description
TRDYn	PCI	Tri-statable OUTPUT	Target ready. Active low signal indicating that PCILite is ready to complete the current transaction.
USR[24:0] or USR[13:0] or USR[5:0]	USER	INPUT/OUTPUT	USER pins: Each pin can individually be software configured to be an INPUT, OUTPUT, or active low chip-select.
VCCA	Power	PCI/USER	Connect to 2.5V. It is recommended that the 2.5V be derived from the PCI slot's 5V rail and not 3.3V rail, because on some systems, the 3.3V rail is not connected.
VCCI	Power	PCI/USER	Connect to 5V
CONT_L	USER	INPUT	User wait pin. When the HOLD mode is enabled, the cycle will stop during the time that WR_L or RD_L is low, (DU period) until a falling edge on this pin is detected (if the HOLD TYPE is EDGE), or until CONT_L is high (if the HOLD TYPE is LEVEL).
WR_L	USER	OUTPUT	User Write pin When low, it indicates that the PCI is doing a write to a valid address of this card. Data and address is valid a programmable time before the falling edge of this signal. The duration of this signal is programmable, to be 30ns, 60ns, 90ns, 120ns, 150ns, 180ns, 210ns etc. up to 480ns, or can be lengthened by the use of the CONT_L signal. The user should note that the use of very slow transfers, violates the PCI specification. This violation of the PCI spec should not cause problems, because PCI bridges allows for much longer delays in transactions.

3. REGISTERS

3.1. MEMORY MAP

In PCILite, all the USER and PCI registers are memory mapped. Below is the memory map for PCILite's 128k memory range.

DESCRIPTION	Mem Range
External Memory	00000/h
	0FFFF/h
User Register Block	10000/h
	10010/h
Not Used	10014/h
	17FFF/h
PCI Registers	18000/h
	18049/h
Not Used	18050/h
	1FFFF/h

3.2. USER REGISTERS

These are internal registers that are specific to PCILite. Their function is explained in the table that follows.

Register name	Address	Description
REG0	10002/h to 10000/h Bits[N:0]	Used in conjunction with REG1, to define the status of the USR pins. Each bit corresponds with a user pin.
REG1	10006/h to 10004/h Bits[N:0]	Used in conjunction with REG0, to define the status of the USR pins. Each bit corresponds with a user pin. For user pin N: where N= 0 to 24,13 or 5 (depending on which bus version is used)
		Reg1[N] Reg0[N] USR[N] Function
		0 0 INPUT
		0 1 ACTIVE low OUTPUT
		1 0 ACTIVE low CHIP-SELECT OUTPUT
1 1 ACTIVE high OUTPUT		
SU[1:0]	10008/h Bits[1:0]	<u>Setup.</u> Specifies how many clock cycles the DATA and ADDRESS lines must be stable before WR_L will go low. The amount of cycles equals to SU + 1. Thus a maximum of 4 clock cycles can be selected, resulting in a time of 240ns.
DU[3:0]	10008/h Bits[7:4]	<u>Duration.</u> Specifies the width of the RD_L or WR_L pulse. The amount of cycles is equal to DU + 1. Thus a maximum of 16 clock cycles can be selected, resulting in a time of 480ns.
HLD[1:0]	10009/h Bits[9:8]	<u>Hold.</u> Specifies how many clock cycles the DATA and ADDRESS lines must be kept stable after WR_L or RD_L will goes high. The amount of cycles is equal to HLD . Thus a maximum of 3 clock cycles can be selected, resulting in a time of 90ns.
HOLD_MODE	10009/h Bit 12	When set, this bit selects a mode that causes the cycle to be stopped just after the RD_L or WR_L signal has gone low. Depending on HOLD_TYPE configuration the cycle continues on a specific state of signal CONT_L. SU, DU and HLD registers are still functional.
HOLD_TYPE	10009/h Bit 13	This register is only used when HOLD MODE is enabled. If this bit is cleared, the HOLD TYPE is set as EDGE: The transfer is completed (RD_L or WR_L goes high 1.5 to 2.5 plus DU clock cycles) when a negative edge on CONT_L has been detected. If this bit is set, the HOLD TYPE is set as LEVEL: The cycle is completed when (RD_L or WR_L goes high 1.5 to 2.5 plus DU clock cycles) when CONT_L is high.
READ_USER	10010/h Bits[N:0] Where N is 24, 13 or 5.	This register is used to read the values of the USER pins.
FORCE_INT	1000C/h Bits[31:0]	Writing ones to this location cause an interrupt to occur. The interrupt must still be enabled before this can take place.

3.3. PCI REGISTERS

The table that follows describes the standard PCI registers that can be modified in PCILite. Not all PCI registers can be modified in PCILite; those that cannot be modified are not described in the table. A full description of all PCI registers can be found in the PCI Local Bus Specification, Revision 2.2.

Address	Name	Function	Note
18001\h and 18000\h Bits [15:0]	Vendor ID	This field identifies the manufacturer of the device. The PCI SIG to ensure uniqueness allocates valid vendor identifiers. 0FFFFh is an invalid value for Vendor ID.	Design specific. Needs to be supplied to ASIC DESIGN SERVICES
18003\h and 18002\h Bits[31:16]	Device ID	This field identifies the particular device. The vendor allocates this identifier.	Design specific. Needs to be supplied to ASIC DESIGN SERVICES
18005\h and 18004\h Bits[15:0]	Command	The command register provides coarse control over a device's ability to generate and respond to PCI cycles. When a 0 is written to this register, the device is logically disconnected from the PCI bus for all accesses except configuration accesses. PCILite supports this base level of functionality. Individual bits in the Command register may or may not be implemented depending on a device's functionality.	See bit description
		PCILite does not implement IO Space and thus does not implement a writeable element at bit location 0 of the command register. PCILite powers up with all 0's in this register.	
		Bit 1: Memory space Controls a device's response to Memory Space accesses. A value of 0 disables the device response. A value of 1 allows the device to respond to Memory Space accesses. State after RST# is 0.	With PCILite this bit is settable
Bit 6	Parity Error response	This bit controls the device's response to parity errors. When the bit is set, the device must take its normal action when a parity error is detected. When the bit is 0, the device sets its Detected Parity Error status bit (bit 15 in the Status register) when an error is detected, but does not assert PERR# and continues normal operation. This bit's state after RST# is 0. Devices that check parity must implement this bit. Devices are still required to generate parity even if parity checking is disabled.	PCILite implements this bit

Address	Name	Function		Note
18005\h and 18004\h Bits[15:0]	Command	Bit 8	SERR Enable This bit is an enable bit for the SERR# driver.	
		All other bits		Permanently tied to 0 on PCILite
18007\h and 18006\h Bits[31:16]	Status	The Status register is used to record information for PCI bus related events. Writes can only cause a bit to be reset, but never set. A one bit is reset whenever the register is written to with a bit in the corresponding bit location.		
		Bit 25 to 26	These bits encode the timing of DEVSEL# . These are encoded as 00b for fast, 01b for medium, and 10b for slow (11b is reserved). These bits are read-only and must indicate the slowest time that a device asserts DEVSEL# for any bus command except Configuration Read and Configuration Write.	PCILite sets them to 01b (Medium)
		Bit 27	A target device must set this bit whenever it terminates a transaction with Target-Abort. Devices that will never signal Target-Abort do not need to implement this bit. PCILite aborts if a read or write is not completed before 30 cycles after the start of a cycle. This violates the PCI specification for targets, but in practice there will be no system problems because PCI bridges can have up to 32 cycles, before a master aborts.	
		Bit 31	The device must set this bit whenever it detects a parity error, even if parity error handling is disabled (as controlled by bit 6 in the Command register).	Implemented on PCILite
		All other bits		Set to 0 on PCILite
18008\h Bits[7:0]	Revision Id	This register specifies a device specific revision identifier. The vendor chooses the value. Zero is an acceptable value. This field should be viewed as a vendor defined extension to the <i>Device ID</i> .		Design specific. Needs to be supplied to ASIC DESIGN SERVICES. The unmodified PCILITE device this is set to 0x21h

Address	Name	Function	Note	
1800B\h to 18009\h Bits[31:8]	Class Code	The Class Code register is read-only and is used to identify the generic function of the device and, in some cases, a specific register-level programming interface. The register is broken into three byte-size fields. Encoding for base class, sub-class, and programming interface are provided for Later. All unspecified encodings are reserved.	Design specific. Needs to be supplied to ASIC DESIGN SERVICES	
18009\h Bits[15:8]	Specific register-level programming interface	Identifies a specific register-level programming interface (if any) so that device independent software can interact with the device.		
1800A\h Bits[23:16]	Sub-class	Sub-class code which identifies more specifically the function of the device.		
1800B\h Bits[31:24]	Base class	The base class code, which broadly classifies the type of function the device performs.		
1800C\h Bits[7:0]	Cache Line Size	This read/write register specifies the system cacheline size in units of DWORDS.	Always set to zero on PCILite	
1800D\h Bits[15:8]	Latency Timer	This register specifies, in units of PCI bus clocks, the value of the Latency Timer for this PCI bus master.	Always set to zero on PCILite	
1800E\h Bits[23:16]	Header Type	This byte identifies the layout of the second part of the predefined header (beginning at byte 10h in Configuration Space) and also whether or not the device contains multiple functions. Bit 7 in this register is used to identify a multi-function device. If the bit is 0, then the device is single function. If the bit is 1, then the device has multiple functions. Bits 6 through 0 identify the layout of the second part of the predefined header. The encoding 00h specifies the layout shown here. The encoding 01h is defined for PCI-to-PCI bridges and is defined in the document <i>PCI to PCI Bridge Architecture Specification</i> . The encoding 02h is defined for a CardBus bridge and is documented in the <i>PC Card Standard</i> . All other encodings are reserved.	PCILite uses encoding 00\h	
18013\h to 18010\h Bits[31:0]	Base Address Register	Specifies where in memory or IO the card will be mapped. Bit 0 in all Base Address registers is read only and is used to determine whether the register maps into memory or IO space. Base Address registers that map to Memory Space must return a 0 in bit 0. Base address registers that map into IO Space must return 1 in bit 0.		
		Bit 0	Species if it is a memory or IO base pointer.	Set to zero on PCILite. (Memory mapped)

Address	Name	Function	Note	
18013\h to 18010\h Bits[31:0]	Base Address Register	Bit 1,2	Type: 00: Locate anywhere in 32-bit space. 01: The encoding to support memory space below 1M was supported in previous versions of the specification. System software should recognize this encoding and handle appropriately. 10: locate anywhere in 64 bit space 11: Reserved.	Set to 00b on PCILite
		Bit3	Prefetchable. Set to one if there are no side effects on reads, the device returns all bytes on reads regardless of the byte enables, and host bridges can merge processor writes to this range without causing errors. Any device that has a range that behaves like normal memory should mark the range as prefetchable. A linear frame buffer in a graphics device is an example of a range that should be marked prefetchable. Bit must be set to zero otherwise.	This bit is set on PCILite.
		Bits 4 to 31	The number of upper bits that a device actually implements depends on how much of the address space the device will respond to. A 32-bit register can be implemented to support a single memory size that is a power of 2 from 16 bytes to 2Gb. A device that wants 1MB memory space would use the top 12 bits of the address register, hardwiring the other bits to 0.	PCILite supports bits 31 down to 17. This gives a space of $2^{17}=128k$ bytes. Half of this space is available externally through $A[13:0] = 2^{14}=16k$ DWORDS=64Kbytes.
18028\h	CardBus CIS Pointer	This is not implemented on PCILite and thus all bits are set to zero.		

Address	Name	Function	Note
1802D\h to 1802C\h Bits[15:0]	Subsystem Vendor ID	<p>These registers are used to uniquely identify the expansion board or subsystem. They provide a mechanism for expansion board vendors to distinguish their boards from one another even though the boards may have the same PCI controller on them. (and therefore, the same Vendor ID and Device ID) Implementation of these registers is required for ALL PCI devices except certain base classes.</p> <p>Values in these registers must be loaded and valid prior to the system BIOS or any systems software accessing the PCI configuration space. Devices are responsible for guaranteeing that data is valid before allowing reads to these registers to complete. This can be done by responding to any accesses with retry until data is valid.</p> <p>A company has only one Vendor ID. That value can be used in either the Vendor ID field of configuration space (offset 00h) or the Subsystem Vendor ID field of configuration space (offset 2Ch). It is used in the Vendor ID field (offset 00h) if the company built the silicon. It is used in the Subsystem Vendor ID field (offset 2Ch) if the company built the add-in card. If a company builds both the silicon and the add-in card, then the same value would be used in both fields.</p>	Design specific. Needs to be supplied to ASIC DESIGN SERVICES
1802F\h to 1802E\h Bits[31:16]	Subsystem ID	See Subsystem Vendor ID	
18034\h Bits[7:0]	Capacity Pointer		These bits are not implemented on PCILite and are all set to zero.
1803C\h Bits[7:0]	Interrupt Line	<p>The Interrupt line register is used to communicate interrupt line routing information. This register is read/write and must be implemented by any device that uses an interrupt pin. POST software will write the routing information in to this register as it initializes and configures the system.</p> <p>The value in this register tells which INPUT of the system interrupt controller(s) the device's interrupt pin is connected to. The device itself does not use this value; device drivers and operating systems use it. Device drivers and operating systems can use this information to determine priority and vector information. Values in this register are system architecture specific.</p>	

Address	Name	Function	Note
1803D\h Bits[15:8]	Interrupt Pin	The interrupt Pin register tells which interrupt pin the device uses. A value of 1 corresponds to INTA#. A value of two corresponds to INTAB#. A value of 3 corresponds to INTC#. A value of 4 corresponds to INTD#. This register is read only.	PCILTE sets it to 1. (INTA#)
1803E\h Bits[23:16]	Min_GNT	Set to zero on PCILite, indicating that the device has no major requirements for the setting of Latency Timers.	
1803F\h Bits[31:24]	Max_LAT	Set to zero on PCILite, indicating that the device has no major requirements for the setting of Latency Timers.	
18049\h and 18048\h	Interrupt control	Bit 8 A '1' in this bit indicates an active external interrupt condition (assertion of EXT_INTn). It is cleared by the user by writing a '1' to this bit position. It is set to '0' after reset.	
		Bit 9: Writing a '1' to this bit enables support for the external interrupt signal. Writing a '0' to this bit disables external interrupt support.	
		All other bits are R/O Reserved and set to '0'.	

4. FUNCTIONAL DESCRIPTION

4.1. THE BURST TRANSACTION

The basic mechanism of data transfer in PCI is the burst transaction.

Write cycle

The master drives IRDY_L (initiator ready) low, when the correct data is placed on the AD[31:0] bus by the master. When the target is ready to receive the data, it drives the TRDY_L (target ready) low.

In zero wait state transfers IRDY_L and TRDY_L will be low, and one transfer can take place every clock cycle. PCILite adds one clock cycle so that the address and data can be stable before the WR_L signal is issued. Additional clock cycles can be specified using the SU register. The length of the WR_L pulse is specified by the DU register, and the Data and address hold is specified by the HLD register.

When the master does not have any more data to write, it pulls the FRAME_L signal high again. The target will remove the DEVSEL_L signal, once it has finished with the transaction.

Read cycle.

The read cycle works in the same way, with the exception that the TARGET will drive the TRDY signal low once it has placed the valid data on the AD[31:0] bus. Data is fetched from an internal register or external location by using the RD_L signal. The SU and HLD registers specify the setup and hold of the external address bus. The DU register specifies the duration of the RD_L signal.

Cycle timing:

Registers SU, DU, HLD, HOLD_MODE and HOLD_TYPE define the cycle timing.

Setup:

Defined as the length of time (in terms of PCI clock cycles) that data/chip-selects and address lines are set up before RD_L or WR_L signals becomes active. This is equal to SU + 1 clock cycles.

Duration:

This is the number of clock cycles RD_L or WR_L will remain active. This is equal to DU+1 clock cycles.

Hold:

The number of clock cycles data/chip-selects and address lines are held active after the rising edge of RD_L or W_L signals. This is equal to HLD clock cycles.

Hold mode:

When this bit is set the cycle stops after RD_L or WR_L signals have gone low. The HOLD_TYPE register then determines how PCILite will respond to a signal on the CONT_L pin.

Warning: Do not enable this mode unless the CONT_L pin is connected to the appropriate circuitry.

Hold type:

This register is only used when HOLD MODE is enabled.

If this bit is cleared, the HOLD TYPE is set as EDGE:

The transfer is completed (RD_L or WR_L goes high 1.5 to 2.5 plus DU clock cycles) when a negative edge on CONT_L has been detected.

If this bit is set, the HOLD TYPE is set as LEVEL:

The cycle is completed when (RD_L or WR_L goes high 1.5 to 2.5 plus DU clock cycles) when CONT_L is high.

The Configuration Register (address 10008/h as seen on page 13) is used to set the above parameters and is the collective name for the 5 above-mentioned registers. In the Configuration Register, the Setup value

occupies bits [1:0], the Duration value occupies bits [7:4], the Hold value occupies bits [9:8], the Hold_mode bit is bit 12 and the Hold_type bit is bit 13.

Bits 3, 5, 7, 11 and 14 - 15 are not used and should be set to 0.

The Configuration register is defined as:

BIT	[15:14]	13	12	[11:10]	[9:8]	[7:4]	[3:2]	[1:0]
USE	n/u	Hold_type	Hold_mode	n/u	Hold	Duration	n/u	Setup

Example:

To set the configuration register so that the Setup time is 3 clock cycles, the Duration is 3 clock cycles, the Hold time is 2 clock cycles and Hold mode is enabled with type EDGE, the configuration register must be set as:

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0	0	0	1	0	0	1	0	0	0	1	0	0	0	1	0

4.2. USER PINS

This section describes the USER pins for the 32-bit PQ208 and 16-bit version of PCILite. The USER pins for the 32-bit TQ144 and 8-bit versions work in the same way, the only difference is that in these versions there are only 14 and 6 USER pins respectively.

Each of the user pins USR[24:0] can be individually software configured to be an INPUT, OUTPUT, or active low chip-select.

REG0 and REG1 define the status of the USR[24:0] pins. Each bit corresponds with a user pin. For N=0 to 24.

REG1[N]	REG0[N]	USR[N] function
0	0	Input
0	1	Active low output
1	0	Active low chip-select output
1	1	Active high output

Example:

To configure the USER Pins with pins 0 – 4 as inputs, pins 5 – 9 as active low outputs, pins 10 – 14 as active low chip-select outputs and pins 15 – 24 as active high outputs, the setup is as follows.

REG0 and REG1 must be set up as:

Bit	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
REG1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
REG0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0

CHIP SELECT

The mapping between PCI addresses and A[13:0] on the PCILite backend is as follows:

$$A[13:0] = \text{PCI address}[15:2]$$

If a user pin is defined as a chip-select then that pin will be active whenever a specific address range is addressed. A[13:9] is decoded to select whether or not a chip select is enabled (in the 8-bit version, A[13:11] is decoded and in the 32-bit TQ144 version, A[13:10] is decoded). So, if USR0 is set as a chip select, it will only be enabled (go low) when A[13:9] = 00000/b, and PCILite is being addressed. Similarly, if USR1 is set as a chip select, it will only be enabled (go low) when A[13:9] = 00001/b, and PCILite is being addressed etc.

Example:

USR[0]

Active (low) when:

- PCI address[31:17] = BASE_ADDR_REG[31:17]. (PCILite is being addressed)
- PCI address[16] = 0\b (User or PCI registers in PCILite are not being addressed)
- PCI address[15:11] = 00\h (A[13:9]=00\h)
- Memory read or write cycle is performed.
- REG0[0]=0\b
- REG1[0]=1\b

In other words, transfers must be made to PCILite BASE_ADDR_REG + 0\h

USR[1]

Active (low) when:

- PCI address[31:17] = BASE_ADDR_REG[31:17]. (PCILite is being addressed)
- PCI address[16] = 0\b (User or PCI registers in PCILite are not being addressed)
- PCI address[15:11] = 00\h (A[13:9]=01\h)
- Memory read or write cycle is performed.
- REG0[1]=0\b
- REG1[1]=1\b

In other words, transfers must be made to PCILite BASE_ADDR_REG + 800\h

USR pin 20 can be selected to serve as a global chip-select (USR pin 5 in 8-bit version and USR pin 13 in the 32-bit TQ144 version). If this is done, then whenever a backend mapped transfer occurs (irrespective of the value of PCI address[15:11]) this signal will become active (low).

Note: Because PCILite uses double word transfers, data can only be written/read from every 4th address, i.e. only address offsets 0h, 4h, 8h, ... etc are valid addresses. This is applicable to both the 8-bit and 32-bit versions.

The table below shows the chip-select function when Reg1=00FFFFFF\h and Reg0=00000000\h, thus, USR[24:0] are all set as chip-selects. The addresses shown are byte addresses. Please note that the backend address is a DWORD address. The chip selects will go low only when a transfer is made to the back-end address space.

Start Address relative to base pointer (Byte)	End Address relative to base pointer (Byte)	User pin.																								
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
0000\h	07FF\h	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1
0800\h	0FFF\h	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1
1000\h	17FF\h	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1
1800\h	1FFF\h	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1
2000\h	27FF\h	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1
2800\h	2FFF\h	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1
3000\h	37FF\h	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1
3800\h	3FFF\h	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1
4000\h	47FF\h	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1
4800\h	4FFF\h	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1
5000\h	57FF\h	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	0	1	1	1	1
5800\h	5FFF\h	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	0	1	1	1	1
6000\h	67FF\h	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0	1	1	1	1
6800\h	6FFF\h	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	0	1	1	1	1
7000\h	77FF\h	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	0	1	1	1	1
7800\h	7FFF\h	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	0	1	1	1	1
8000\h	87FF\h	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	0	1	1	1	1
8800\h	8FFF\h	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	0	1	1	1	1	1
9000\h	97FF\h	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0	1	1	1	1	1
9800\h	9FFF\h	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	1	1	1	1
A000\h	A7FF\h	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1
A800\h	AFFF\h	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	1	1	1
B000\h	B7FF\h	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0	1	1
B800\h	BFFF\h	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	0	1
C000\h	CFFF\h	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	0
D000\h	FFFF\h	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1

Note: The above table describes the 32-bit PQ208 and 16-bit versions of PCILite. The 32-bit TQ144 version operates in the same way, except that there are only 14 USER pins and the block size is bigger, 4096 bytes (as opposed 2048 bytes for the 32-bit PQ208 and 16-bit versions). Similarly in the 8-bit version there are only 6 USER pins and the block size is 8192 bytes.

The table below shows the OUTPUT of function when Reg1=00FFFFFFE\h and Reg0=00000101\h, thus USR0 is an active low output, USR8 is an active high output and all the other USR pins are chip-selects. The addresses shown are byte addresses. Please note that the backend address is a DWORD address. The chip selects will go low only when a transfer is made to the back-end address space. When a pin is selected as an INPUT or OUTPUT it stays at this level once it has been set.

Start Address relative to base pointer (Byte)	End Address relative to base pointer (Byte)	User pin.																								
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
0000\h	07FF\h	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1
0800\h	0FFF\h	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1
1000\h	17FF\h	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1
1800\h	1FFF\h	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1
2000\h	27FF\h	0	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1
2800\h	2FFF\h	0	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1
3000\h	37FF\h	0	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1
3800\h	3FFF\h	0	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1
4000\h	47FF\h	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1
4800\h	4FFF\h	0	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1
5000\h	57FF\h	0	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	0	1	1	1	1
5800\h	5FFF\h	0	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	0	1	1	1	1
6000\h	67FF\h	0	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	0	1	1	1	1
6800\h	6FFF\h	0	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	0	1	1	1	1
7000\h	77FF\h	0	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	0	1	1	1	1
7800\h	7FFF\h	0	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0	1	1	1	1
8000\h	87FF\h	0	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	0	1	1	1	1
8800\h	8FFF\h	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	0	1	1	1	1
9000\h	97FF\h	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	0	1	1	1	1
9800\h	9FFF\h	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	0	1	1	1	1
A000\h	A7FF\h	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1
A800\h	AFFF\h	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	1	1	1
B000\h	B7FF\h	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0	1	1
B800\h	BFFF\h	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	0	1
C000\h	CFFF\h	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	0
D000\h	FFFF\h	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1

Note: The above table describes the 32-bit PQ208 and 16-bit versions of PCILite. The 32-bit TQ144 version operates in the same way, except that there are only 14 USER pins and the block size is bigger, 4096 bytes (as opposed 2048 bytes for the 32-bit PQ208 and 16-bit versions). Similarly in the 8-bit version there are only 6 USER pins and the block size is 8192 bytes.

4.3 INTERRUPT PIN

PCILite has a single edge triggered interrupt pin. A falling edge on this pin will cause INTAN to go low (If interrupts are enabled on PCILite). Interrupts are cleared using the dedicated PCI register contained within PCILite.

To enable the interrupt pin, the Interrupt Control Register is used, by setting bit 9 to a '1'; the external interrupt pin is enabled. If an interrupt then occurs on this pin, bit 8 is set to a '1' by PCILite to indicate that there has been an interrupt. Once an interrupt has occurred, bit 8 must be cleared by the user, this is done by writing a '1' to bit 8. The address of the Interrupt Control Register and its full description can be found on page 19.

An interrupt can also be forced by writing ones the FORCE_INT register.

4.4 BACKEND INTERFACE

The backend consist of an address and bi-directional data bus. Active low Read (RD_L) and write (WR_L) signals are provided.

When the HOLD_MODE is enabled, data transfers are started but during the time that RD_L or WR_L is active PCILite waits for a falling edge on signal CONT_L (If HOLD_TYPE is "0"), or for CONT_L to be high (If HOLD_TYPE is "1") before continuing with the cycle. This mode is useful when interfacing with devices, that might not be ready when the PCI bus wants to make transfers.

Read and write cycle timing is a function of the Configuration Register (made up of 5 registers as previously mentioned) and the CONT_L pin. The following timing diagrams illustrate the operation of the backend interface.

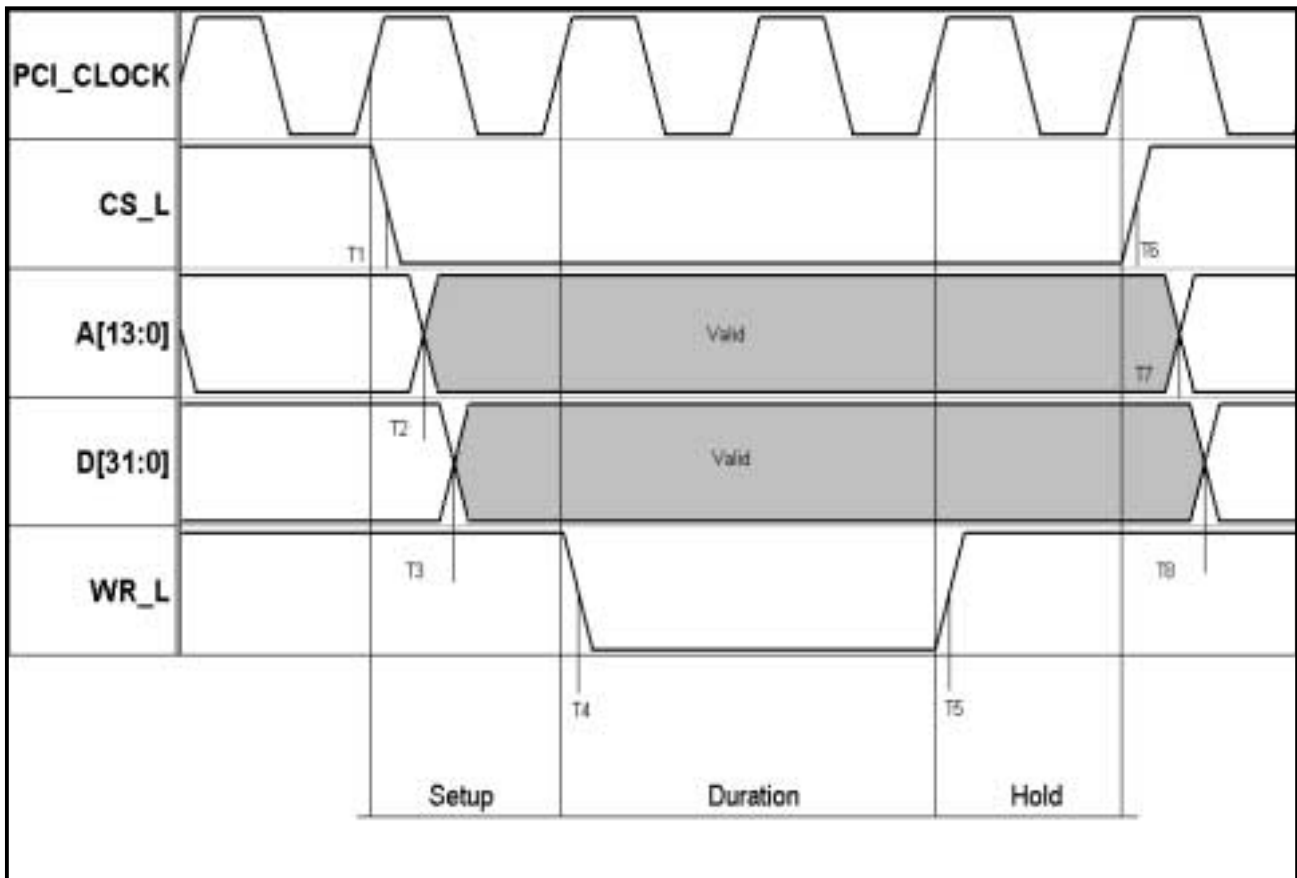


Figure 1. Backend Write timing when SU = 0; DU = 1; HLD = 1.

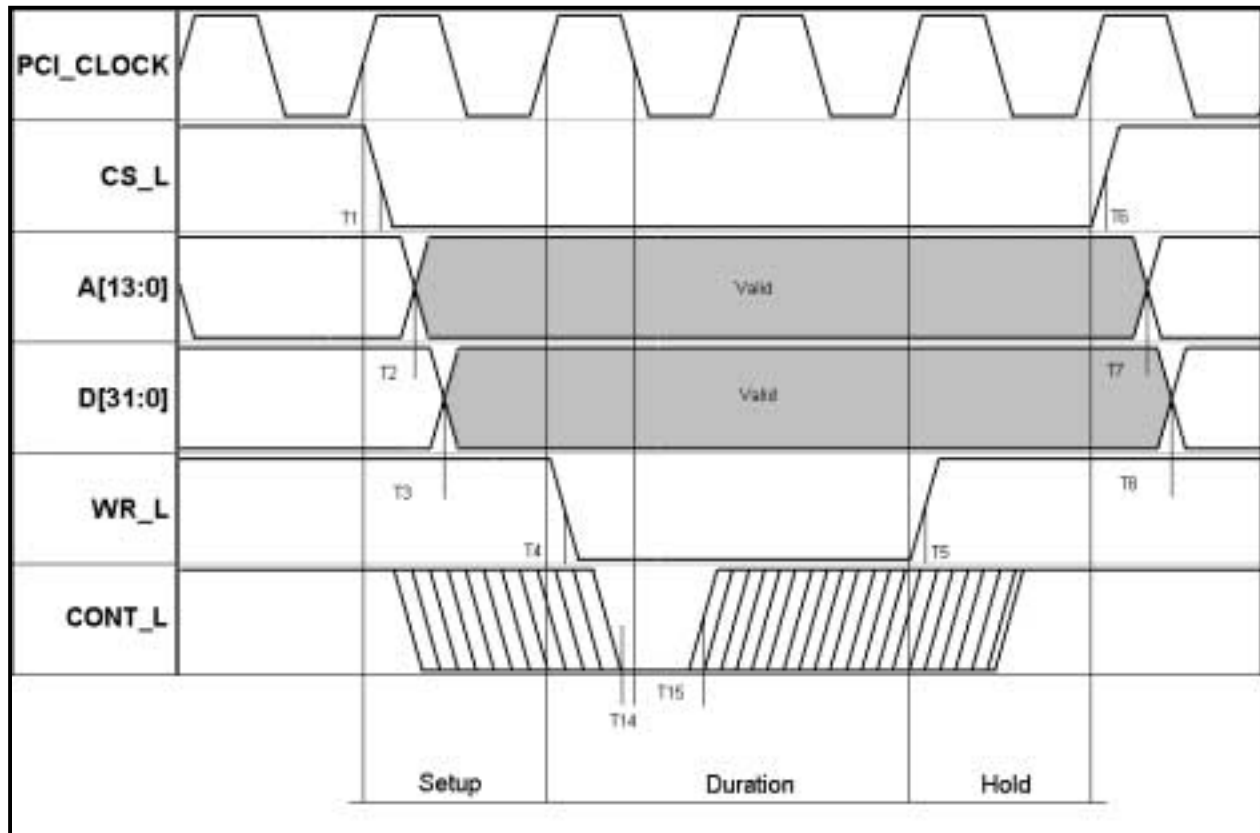


Figure 2. Backend Write timing using the CONT_L signal (with EDGE Hold_type), when SU = 0; DU = 1; HLD = 1.

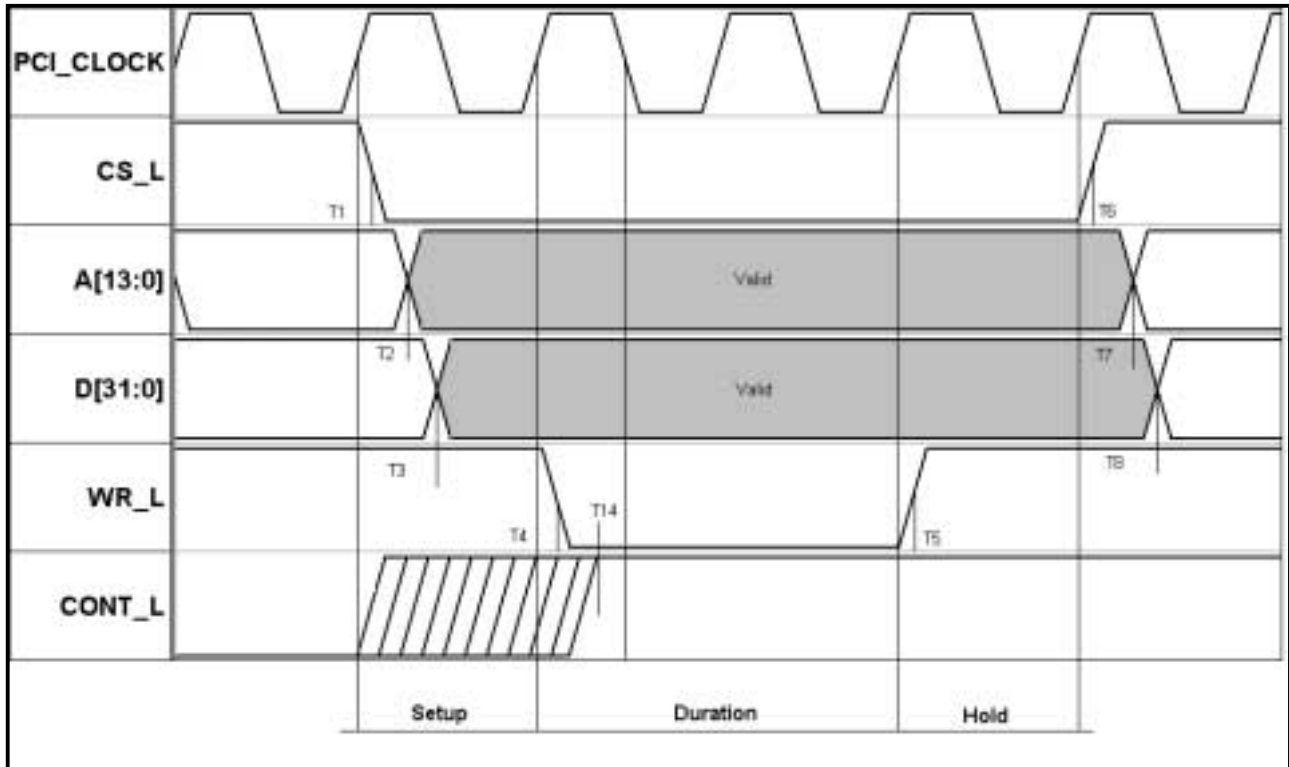


Figure 3. Backend Write timing using the CONT_L signal (with LEVEL Hold_type), when SU = 0; DU = 1; HLD = 1.

The CONT_L signal is used when PCILite is connected to relatively slow device. Typically it would be connected to a signal that indicates whether or not the device is ready for a read/write.

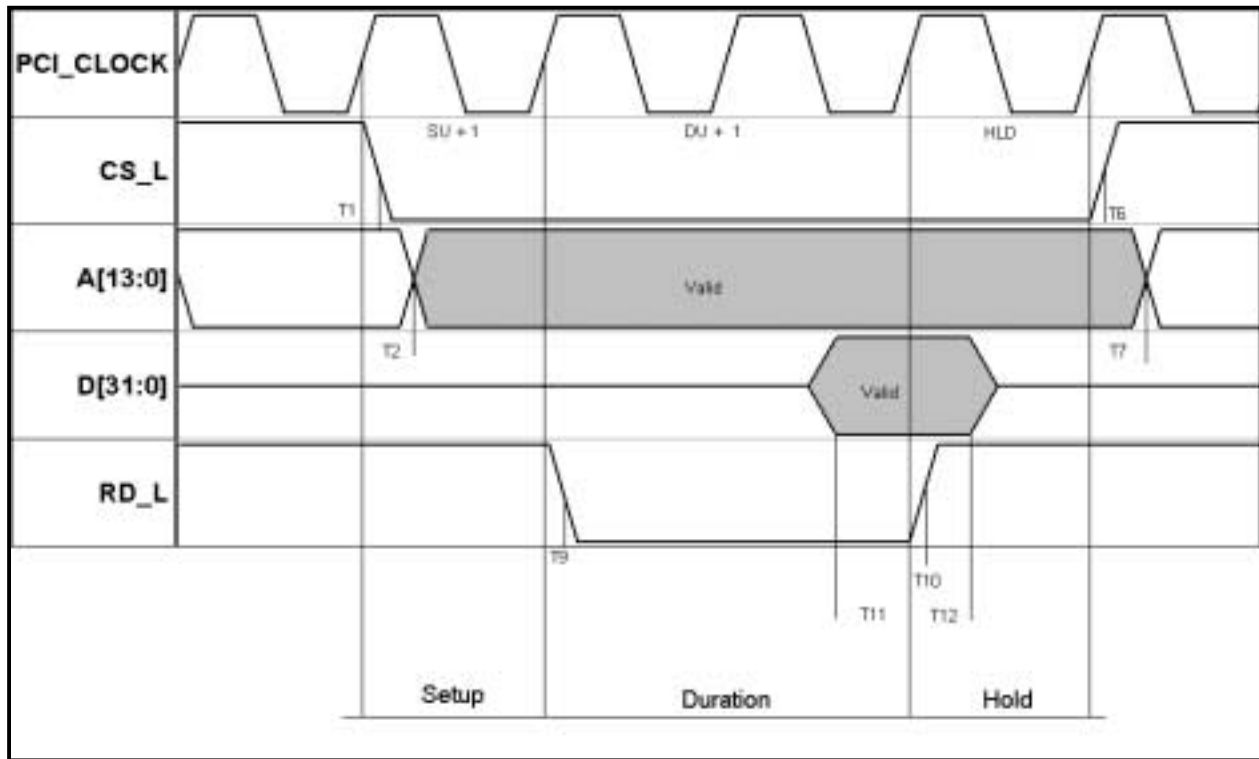


Figure 4. Backend Read timing, when SU = 0; DU = 1; HLD = 1.

Note: Because PCILite uses double word transfers, data can only be written/read from every 4th address, i.e. only address offsets 0h, 4h, 8h, ... etc are valid addresses.

Timing values

Signal	Min	Max	Units
T1	7.3	14.6	ns
T2	4.5	8.9	ns
T3	6.7	13.7	ns
T4	3.8	7.4	ns
T5	3.8	7.4	ns
T6	7.3	14.6	ns
T7	4.5	8.9	ns
T8	6.7	13.7	ns
T9	3.8	7.4	ns
T10	3.8	7.4	ns
T11 (Setup)	0.7	1.5	ns
T12 (Hold)	-0.2	-0.6	ns
T14 (Setup)	0.3	0.7	ns
T15 (Hold)	0.3	0.5	ns

5. TIMING DIAGRAMS

PCILite responds within one clock cycle to the frame signal. This is the fastest any PCI device can respond to the FRAME signal, resulting in a minimum latency

The maximum throughput PCILite can handle is $33\text{Mhz} \times 4 \text{ Byte} / 2 \text{ cycle} = 66\text{Mbyte/sec}$.

Number of cycle needed to transfer N Double words = $3 + (2 + \text{SU} + \text{DU} + \text{HLD}) \times \text{N}$.

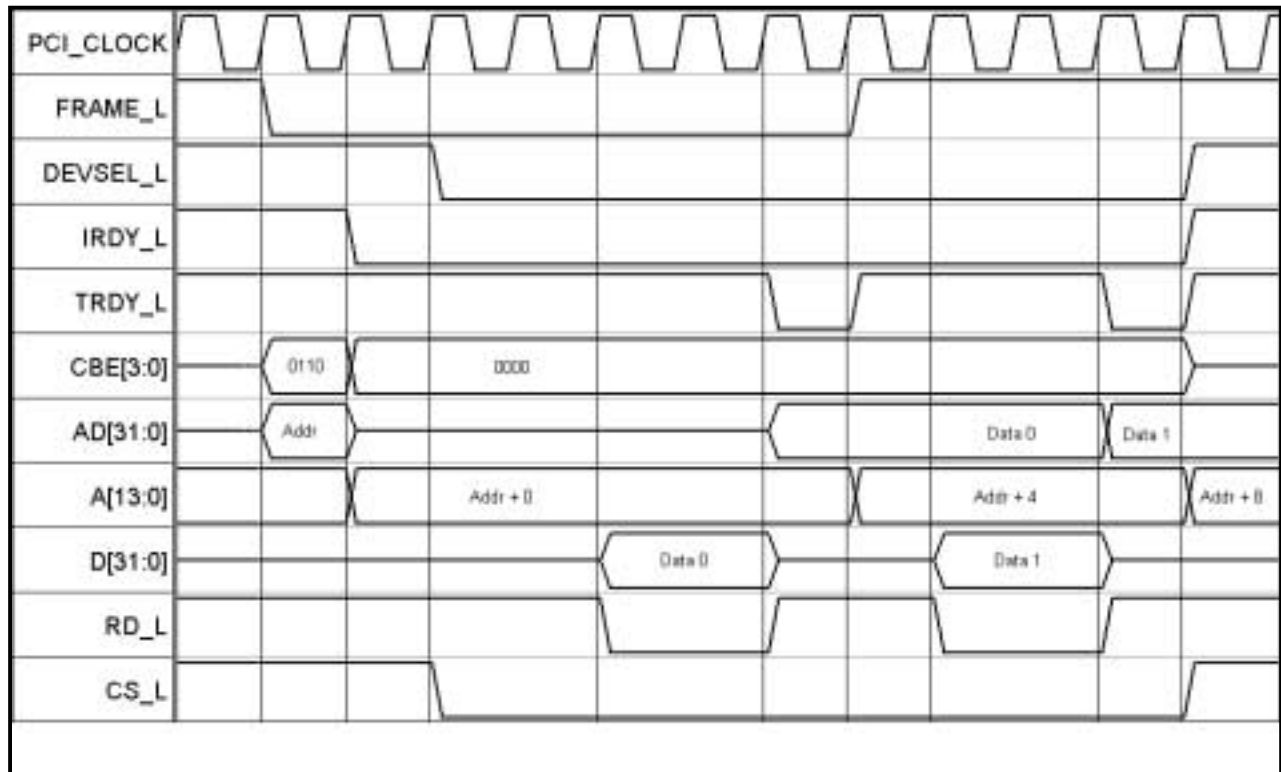


Figure 5. PCILite Read timing when SU = 0, DU = 1 and HLD = 1.

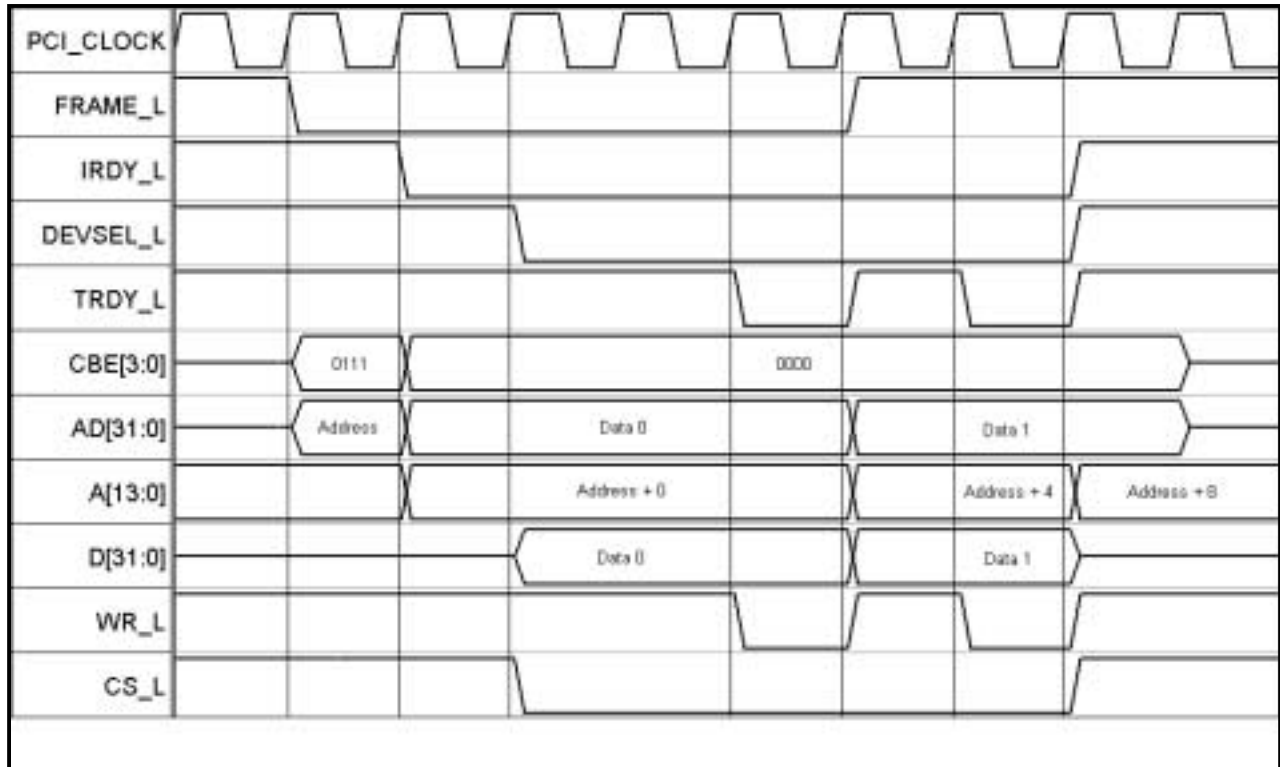


Figure 6. PCILite Write timing when SU = 0, DU = 0 and HLD = 0.

6. PACKAGE AND PINOUT DETAILS

6.1. PACKAGE DETAILS

PCILite is available in an 8-bit, 16-bit or a 32-bit version. The standard package for the 8-bit version is a 100TQFP, and for the 16-bit version the standard package is a 144TQFP. The 32-bit version is available in either a 208PQFP or 144TQFP package.

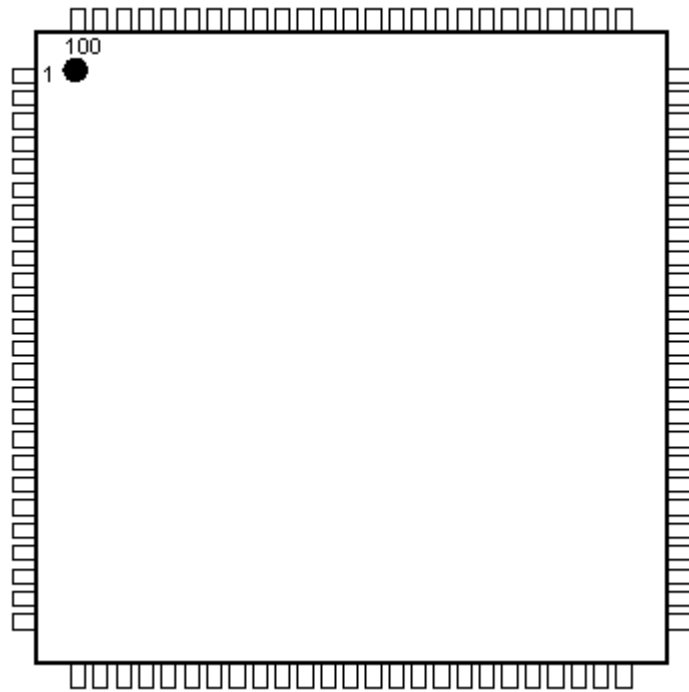


Figure 7. TQFP 100 package footprint.

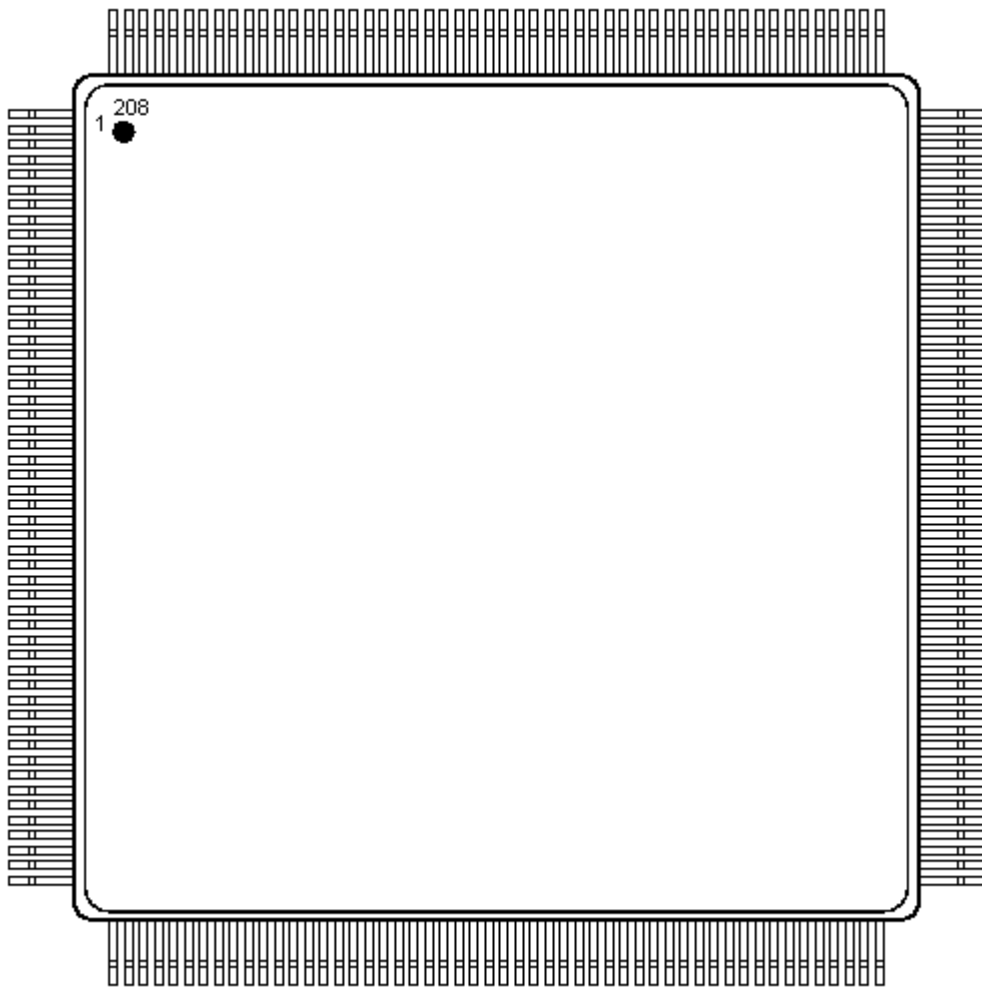


Figure 8. PQFP 208 package footprint.

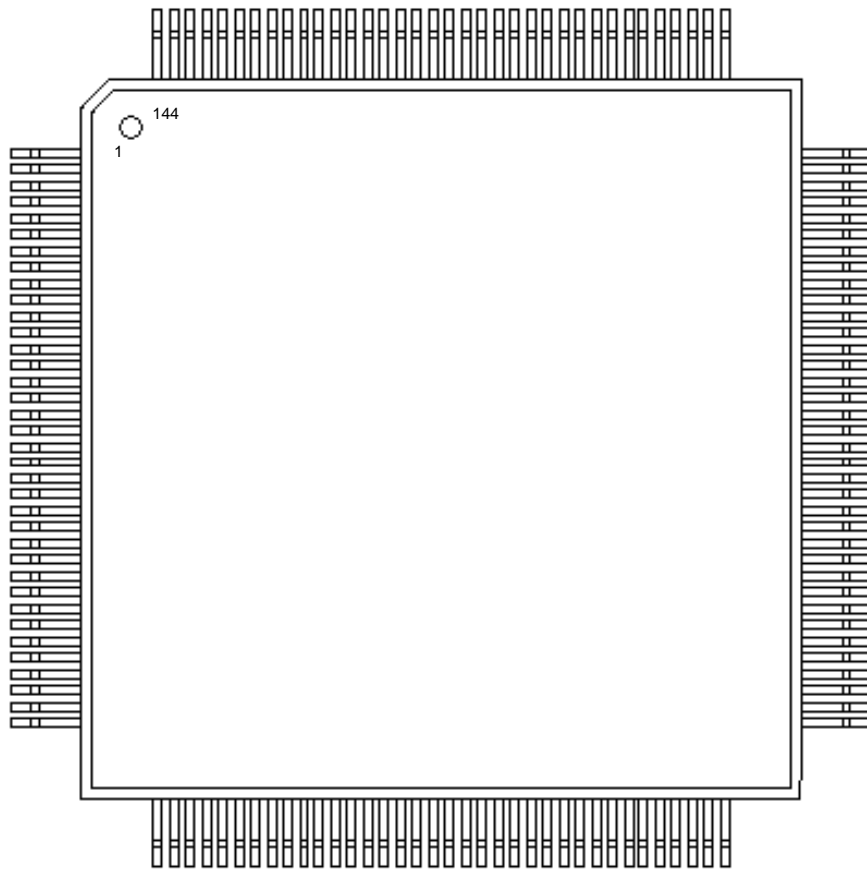


Figure 9. TQFP 144 package footprint.

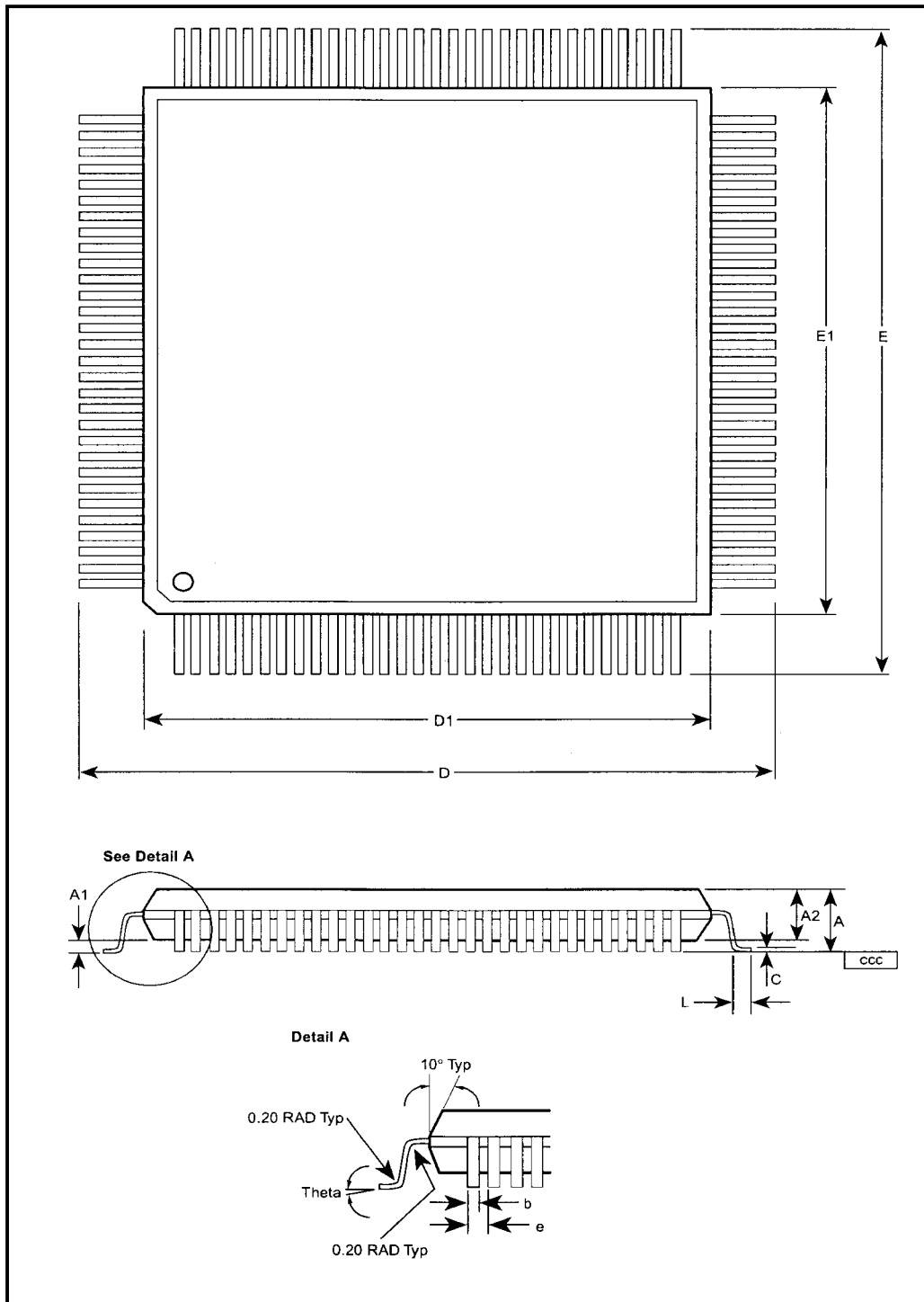


Figure 10. Mechanical characteristics of the TQFP 100, 144 and PQFP 208 packages.

The table below contains the values for the previously mentioned variables. All the dimensions are in millimeters.

Package	TQFP 100			TQFP 144			PQFP 208		
Dimension	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max
A			1.6			1.6		3.7	4.1
A1	0.05	0.10	0.15	0.05	0.10	0.15	0.25	0.38	
A2	1.35	1.40	1.45	1.35	1.40	1.45	3.20	3.40	3.60
b	0.17		0.27	0.17		0.27	0.17		0.27
c	0.09		0.20	0.09		0.20	0.09		0.20
D/E	15.75	16.00	16.25	21.75	22.00	22.25	30.35	30.60	30.85
D1/E1	13.90	14.00	14.10	19.90	20.00	20.10	27.90	28.00	28.10
e	0.50 Basic Spacing between Centers			0.50 Basic Spacing between Centers			0.50 Basic Spacing between Centers		
L	0.45	0.60	0.75	0.45	0.60	0.75	0.50	0.60	0.75
ccc			0.10			0.10			0.10
Theta	0		7 deg	0		7 deg	0		7 deg

6.2. PINOUTS

PCILite 8-bit 100 TQFP

Pin no	Name	Type
1	GND	Power
2	D1	User
3	D0	User
4	USR5	User
5	USR4	User
6	USR3	User
7	TMS	Note 1
8	VCCI	Power
9	GND	Power
10	USR2	User
11	USR1	User
12	USR0	User
13	RD_L	User
14	WR_L	User
15	CONT_L	User
16	INTR_L	User
17	A13	User
18	A12	User
19	A11	User
20	VCCI	Power
21	A10	User
22	A9	User
23	A8	User
24	A7	User
25	A6	User
26	A5	User
27	A4	User
28	A3	User
29	A2	User
30	A1	User
31	A0	User
32	INTAN	PCI
33	AD31	PCI
34	AD30	PCI
35	VCCA	Power
36	GND	Power
37	NC	Not connected
38	AD29	PCI
39	CLK	PCI
40	AD28	PCI

Pin no	Name	Type
41	AD27	PCI
42	AD26	PCI
43	AD25	PCI
44	VCCI	Power
45	AD24	PCI
46	CBE3	PCI
47	IDSEL	PCI
48	AD23	PCI
49	AD22	PCI
50	AD21	PCI
51	GND	Power
52	AD20	PCI
53	AD19	PCI
54	AD18	PCI
55	AD17	PCI
56	AD16	PCI
57	VCCA	Power
58	VCCI	Power
59	CBE2	PCI
60	FRAMEN	PCI
61	IRDYN	PCI
62	TRDYN	PCI
63	DEVSELN	PCI
64	STOPN	PCI
65	PERRN	PCI
66	SERRN	PCI
67	VCCA	Power
68	GND	Power
69	GND	Power
70	PAR	PCI
71	CBE1	PCI
72	AD15	PCI
73	AD14	PCI
74	AD13	PCI
75	AD12	PCI
76	AD11	PCI
77	AD10	PCI
78	AD9	PCI
79	AD8	PCI
80	CBE0	PCI

PCILite 8-bit 100 TQFP (continued)

Pin no	Name	Type
81	AD7	PCI
82	VCCI	Power
83	AD6	PCI
84	AD5	PCI
85	AD4	PCI
86	AD3	PCI
87	GND	Power
88	RSTN	PCI
89	NC	Not connected
90	VCCA	Power

Pin no	Name	Type
91	GND	Power
92	AD2	PCI
93	AD1	PCI
94	AD0	PCI
95	D7	User
96	D6	User
97	D5	User
98	D4	User
99	D3	User
100	D2	User

Note 1: The TMS pin is a test mode pin in Actel's SXA family and should be permanently tied to VCCI.

PCILite 16-bit 144 TQFP

Pin no	Name	Use
1	GND	Power
2	NC	User
3	A2	User
4	A3	User
5	A4	User
6	A5	User
7	A6	Not connected
8	A7	Not connected
9	TMS	Note 1
10	VCCI	Power
11	GND	Power
12	A8	Not connected
13	A9	Not connected
14	A10	Not connected
15	A11	User
16	A12	User
17	A13	User
18	CONT_L	User
19	NC	Not connected
20	VCCA	Power
21	INTR_L	User
22	NC	User
23	RD_L	User
24	WR_L	User
25	USR0	User
26	USR1	User
27	USR2	User
28	GND	Power
29	VCCI	Power
30	VCCA	Power
31	USR3	User
32	USR4	User
33	USR5	User
34	USR6	User
35	USR7	User
36	GND	Power
37	USR8	User
38	USR9	User
39	USR10	User
40	USR11	User

Pin no	Name	Use
41	USR12	User
42	USR13	User
43	USR14	User
44	VCCI	Power
45	USR15	User
46	USR16	User
47	USR17	User
48	USR18	User
49	USR19	User
50	USR20	User
51	USR21	User
52	USR22	User
53	USR23	User
54	NC	User
55	USR24	User
56	VCCA	Power
57	GND	Power
58	NC	Not connected
59	INTAN	PCI
60	CLK	PCI
61	AD31	PCI
62	AD30	PCI
63	AD29	PCI
64	AD28	PCI
65	AD27	PCI
66	AD26	PCI
67	AD25	PCI
68	VCCI	Power
69	AD24	PCI
70	CBE3	PCI
71	IDSEL	PCI
72	AD23	PCI
73	GND	Power
74	AD22	PCI
75	AD21	PCI
76	AD20	PCI
77	AD19	PCI
78	AD18	PCI
79	VCCA	Power
80	VCCI	Power

PCILite 16-bit 144 TQFP (continued)

Pin no	Name	Use
81	GND	Power
82	AD17	PCI
83	AD16	PCI
84	CBE2	PCI
85	FRAMEN	PCI
86	IRDYN	PCI
87	TRDYN	PCI
88	DEVSELN	PCI
89	VCCA	Power
90	NC	Not connected
91	STOPN	PCI
92	PERRN	PCI
93	SERRN	PCI
94	PAR	PCI
95	CBE1	PCI
96	AD15	PCI
97	AD14	PCI
98	VCCA	Power
99	GND	Power
100	AD13	PCI
101	GND	Power
102	VCCI	Power
103	AD12	PCI
104	AD11	PCI
105	AD10	PCI
106	AD9	PCI
107	AD8	PCI
108	CBE0	PCI
109	GND	Power
110	AD7	PCI
111	AD6	PCI
112	AD5	PCI

Pin no	Name	Use
113	AD4	PCI
114	AD3	PCI
115	VCCI	Power
116	AD2	PCI
117	AD1	PCI
118	AD0	PCI
119	D0	User
120	D1	User
121	D2	User
122	D3	User
123	D4	User
124	D5	User
125	GND	Power
126	RSTN	PCI
127	NC	Not connected
128	GND	Power
129	VCCA	Power
130	D6	User
131	NC	User
132	D7	User
133	D8	User
134	D9	User
135	D10	User
136	D11	User
137	D12	User
138	D13	User
139	D14	User
140	VCCI	Power
141	D15	User
142	A0	User
143	A1	User
144	NC	User

Note 1: The TMS pin is a test mode pin in Actel's SXA family and should be permanently tied to VCCI.

PCILite 32-bit 144 TQFP

Pin no	Name	Use
1	GND	Power
2	A11	User
3	A10	User
4	A9	User
5	A8	User
6	A7	User
7	A6	User
8	A5	User
9	TMS	Note 1
10	VCCI	Power
11	GND	Power
12	A4	User
13	A3	User
14	A2	User
15	A1	User
16	A0	User
17	D0	User
18	D1	User
19	NC	Not connected
20	VCCA	Power
21	D2	User
22	D3	User
23	D4	User
24	D5	User
25	D6	User
26	D7	User
27	D8	User
28	GND	Power
29	VCCI	Power
30	VCCA	Power
31	D9	User
32	D10	User
33	D11	User
34	D12	User
35	D13	User
36	GND	Power
37	D14	User
38	D15	User
39	D16	User
40	D17	User

Pin no	Name	Use
41	D18	User
42	D19	User
43	D20	User
44	VCCI	Power
45	D21	User
46	D22	User
47	D23	User
48	D24	User
49	D25	User
50	D26	User
51	D27	User
52	D28	User
53	D29	User
54	D30	User
55	D31	User
56	VCCA	Power
57	GND	Power
58	NC	Not connected
59	INTAN	PCI
60	CLK	PCI
61	AD31	PCI
62	AD30	PCI
63	AD29	PCI
64	AD28	PCI
65	AD27	PCI
66	AD26	PCI
67	AD25	PCI
68	VCCI	Power
69	AD24	PCI
70	CBE3	PCI
71	IDSEL	PCI
72	AD23	PCI
73	GND	Power
74	AD22	PCI
75	AD21	PCI
76	AD20	PCI
77	AD19	PCI
78	AD18	PCI
79	VCCA	Power
80	VCCI	Power

PCILite 32-bit 144 TQFP (continued)

Pin no	Name	Use
81	GND	Power
82	AD17	PCI
83	AD16	PCI
84	CBE2	PCI
85	FRAMEN	PCI
86	IRDYN	PCI
87	TRDYN	PCI
88	DEVSELN	PCI
89	VCCA	Power
90	NC	Not connected
91	STOPN	PCI
92	PERRN	PCI
93	SERRN	PCI
94	PAR	PCI
95	CBE1	PCI
96	AD15	PCI
97	AD14	PCI
98	VCCA	Power
99	GND	Power
100	AD13	PCI
101	GND	Power
102	VCCI	Power
103	AD12	PCI
104	AD11	PCI
105	AD10	PCI
106	AD9	PCI
107	AD8	PCI
108	CBE0	PCI
109	GND	Power
110	AD7	PCI
111	AD6	PCI
112	AD5	PCI

Pin no	Name	Use
113	AD4	PCI
114	AD3	PCI
115	VCCI	Power
116	AD2	PCI
117	AD1	PCI
118	AD0	PCI
119	USR0	User
120	USR1	User
121	USR2	User
122	USR3	User
123	USR4	User
124	USR5	User
125	GND	Power
126	RSTN	PCI
127	NC	Not connected
128	GND	Power
129	VCCA	Power
130	USR6	User
131	USR7	User
132	USR8	User
133	USR9	User
134	USR10	User
135	USR11	User
136	USR12	User
137	USR13	User
138	WR_L	User
139	RD_L	User
140	VCCI	Power
141	CONT_L	User
142	INTR_L	User
143	A13	User
144	A12	User

Note 1: The TMS pin is a test mode pin in Actel's SXA family and should be permanently tied to VCCI.

PCILite 32-bit 208 PQFP

Pin no	Name	Type
1	GND	Power
2	NC	Not connected
3	AD14	PCI
4	NC	Not connected
5	AD13	PCI
6	NC	Not connected
7	AD12	PCI
8	AD11	PCI
9	AD10	PCI
10	AD9	PCI
11	TMS	Note 1
12	VCCI	Power
13	AD8	PCI
14	NC	Not connected
15	CBE0	PCI
16	AD7	PCI
17	NC	Not connected
18	AD6	PCI
19	AD5	PCI
20	NC	Not connected
21	AD4	PCI
22	AD3	PCI
23	NC	Not connected
24	AD2	PCI
25	NC	Not connected
26	GND	Power
27	VCCA	Power
28	GND	Power
29	AD1	PCI
30	AD0	PCI
31	NC	Not connected
32	A13	User
33	A12	User
34	A11	User
35	NC	Not connected
36	A10	User
37	A9	User
38	A8	User
39	NC	Not connected
40	VCCI	Power
41	VCCA	Power
42	A7	User
43	A6	User
44	A5	User
45	A4	User

Pin no	Name	Type
46	A3	User
47	A2	User
48	NC	Not connected
49	A1	User
50	NC	Not connected
51	A0	User
52	GND	Power
53	RD_L	User
54	WR_L	User
55	CONT_L	User
56	D31	User
57	D30	User
58	D29	User
59	D28	User
60	VCCI	Power
61	NC	Not connected
62	D27	User
63	D26	User
64	NC	Not connected
65	NC	Not connected
66	D25	User
67	NC	Not connected
68	D24	User
69	D23	User
70	NC	Not connected
71	D22	User
72	D21	User
73	NC	Not connected
74	D20	User
75	NC	Not connected
76	NC	Not connected
77	GND	Power
78	VCCA	Power
79	GND	Power
80	NC	Not connected
81	D19	User
82	CLK	PCI
83	D18	User
84	D17	User
85	NC	Not connected
86	D16	User
87	D15	User
88	NC	Not connected
89	D14	User
90	D13	User

PCILite 32-bit 208 PQFP (continued)

Pin no	Name	Type
91	NC	Not connected
92	D12	User
93	D11	User
94	NC	Not connected
95	D10	User
96	D9	User
97	NC	Not connected
98	VCCI	Power
99	D8	User
100	D7	User
101	D6	User
102	D5	User
103	NC	Not connected
104	D4	User
105	GND	Power
106	NC	Not connected
107	D3	User
108	NC	Not connected
109	D2	User
110	D1	User
111	D0	User
112	INTR_L	User
113	USR24	User
114	VCCA	Power
115	VCCI	Power
116	NC	Not connected
117	USR23	User
118	USR22	User
119	NC	Not connected
120	USR21	User
121	USR20	User
122	NC	Not connected
123	USR19	User
124	USR18	User
125	NC	Not connected
126	USR17	User
127	USR16	User
128	USR15	User
129	GND	Power
130	VCCA	Power
131	GND	Power
132	NC	Not connected
133	USR14	User
134	USR13	User
135	NC	Not connected

Pin no	Name	Type
136	USR12	User
137	USR11	User
138	NC	Not connected
139	USR10	User
140	USR9	User
141	NC	Not connected
142	USR8	User
143	NC	Not connected
144	USR7	User
145	VCCA	Power
146	GND	Power
147	USR6	User
148	VCCI	Power
149	USR5	User
150	USR4	User
151	USR3	User
152	USR2	User
153	USR1	User
154	USR0	User
155	NC	Not connected
156	NC	Not connected
157	GND	Power
158	SERRN	PCI
159	AD31	PCI
160	AD30	PCI
161	AD29	PCI
162	AD28	PCI
163	AD27	PCI
164	VCCI	Power
165	AD26	PCI
166	AD25	PCI
167	NC	Not connected
168	AD24	PCI
169	CBE3	PCI
170	NC	Not connected
171	IDSEL	PCI
172	INTAN	PCI
173	NC	Not connected
174	AD23	PCI
175	AD22	PCI
176	NC	Not connected
177	AD21	PCI
178	AD20	PCI
179	AD19	PCI
180	RSTN	PCI

PCILite 32-bit 208 PQFP (continued)

Pin no	Name	Type
181	GND	Power
182	NC	Not connected
183	GND	Power
184	VCCA	Power
185	GND	Power
186	NC	Not connected
187	AD18	PCI
188	AD17	PCI
189	NC	Not connected
190	AD16	PCI
191	CBE2	PCI
192	NC	Not connected
193	FRAMEN	PCI
194	IRDYN	PCI

Pin no	Name	Type
195	NC	Not connected
196	TRDYN	PCI
197	DEVSELN	PCI
198	NC	Not connected
199	STOPN	PCI
200	PERRN	PCI
201	VCCI	Power
202	NC	Not connected
203	NC	Not connected
204	PAR	PCI
205	NC	Not connected
206	CBE1	PCI
207	AD15	PCI
208	NC	Not connected

Note 1: The TMS pin is a test mode pin in Actel's SXA family and should be permanently tied to VCCI.

7. APPLICATION EXAMPLE

The example shown below illustrates how to connect PCILite to a dual port RAM device. In this case, PCILite is set up in the HOLD Mode, with the HOLD_TYPE set as EDGE. In this example, CONT_L will be high when RD_L or WR_L is low and BUSY_L_L (dual port RAM signal), which indicates that the RAM is busy and not ready for a read/write. It works as follows. If there is a falling edge on WR_L or RD_L and BUSY_L_L is high, then a falling edge occurs on CONT_L and PCILite continues the cycle. If however there is a falling edge on WR_L or RD_L and BUSY_L_L is low, then CONT_L will be high and PCILite will stop the cycle. When BUSY_L_L goes low, indicating that the RAM is ready for a read/write, there will be a falling edge on CONT_L and PCILite will continue the cycle. By selecting HOLD_TYPE to be LEVEL the BUSY_L_L signal can be directly connected to CONT_L. The external gates will then not be needed.

The dual port RAM device will operate with the delays specified by SU, DU and HLD. For a 75ns SRAM device for example, one should set SU=0, DU=2 and HLD = 0 or 1. It is safer to set HLD up to 1. USR20 must be set up for chip-select in this example.

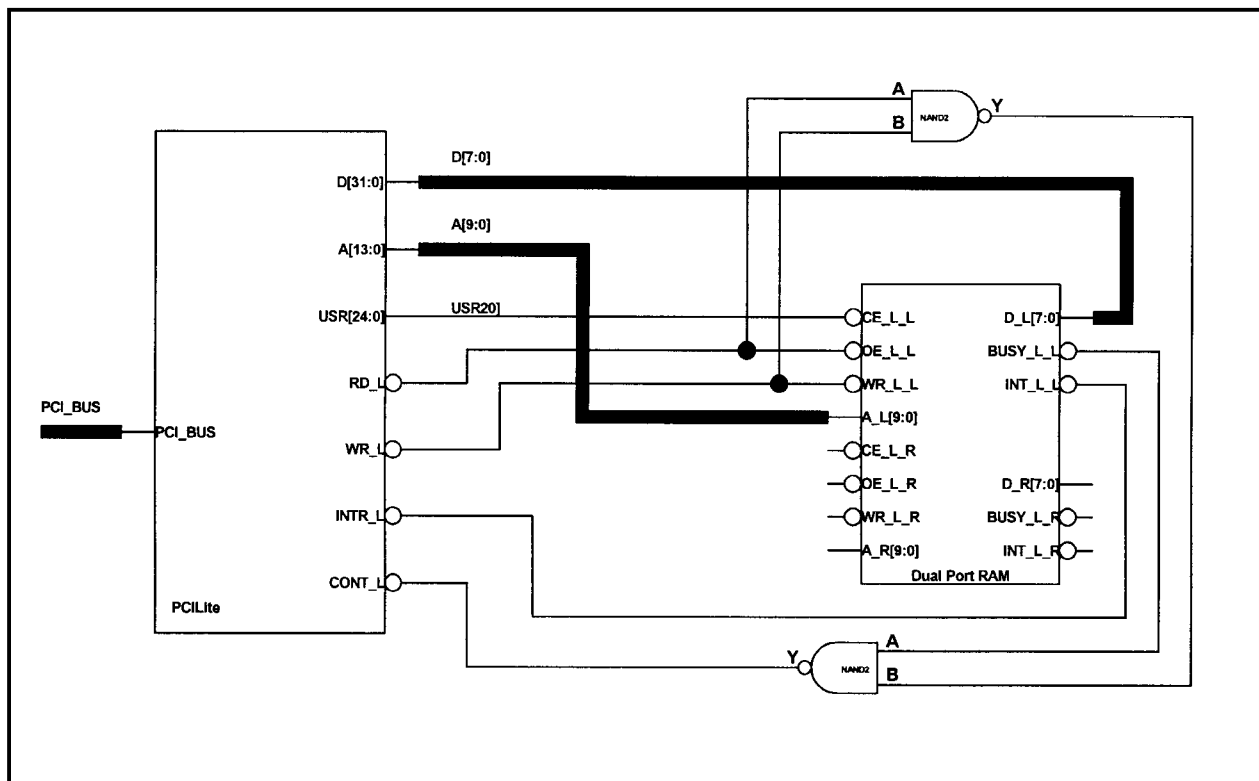


Figure 11. PCILite connected to a dual port RAM.

8. PCI COMPLIANCE

PCILite is fully compliant with the PCI 2.2 Specification however there are a few notes that the user should be aware of.

The Target timeout has been extended to 30 cycles. This allows for a slower backend interface. PCI bridges have a timeout of 32 cycles, and thus a target with a timeout of 30 cycles will work properly. PCILite does not have to be set up so that it times out, and thus can operate in a fully compliant fashion.

The PCI specification specifies 8 clocks between successive TRDY_L signals. Thus the specification will still be met if $SU+DU+HLD+2 < 9$. E.g. $SU=1$, $DU=3$ $HLD=2$ will meet the PCI specification. This will result in data and address set up for two clock cycles, and the WR_L and RD_L pulse being 4 clocks long.

If $SU=4$ $DU=16$ and $HLD=3$ then the successive TRDY_L signals will take 23 clock cycles. PCILite will not terminate with Retry, thus it will work but it does violate the PCI specification.

When using the HOLD mode, PCILite can terminate with retry.

PCILite supports Memory read (0110) and write (0111) only. The memory read command is used to read data in memory-mapped address space. PCILite decodes the top 16 bits ($A[31:17]$) of the 32 bit address space. Address bit 16 is used to select the internal registers in PCILite. External transfers are done when $A16 = 0$. The 64kByte space can be located anywhere in 32-bit address space.

PCILite meets the PCI timing requirements for OUTPUT valid (11ns for 33MHz) and input setup (7ns for 33MHz)

9. OPERATIONAL SPECIFICATION

9.1. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Limits	Units
V _{CCI}	DC Supply Voltage	-0.3 to +6.0	V
V _{CCA}	DC Supply Voltage	-0.3 to +3.0	V
V _I	Input Voltage	-0.5 to +5.5	V
V _O	Output Voltage	-0.5 to +V _{CCI} + 0.5	V
I _{IO}	I/O Source Sink Current ₂	-30 to +5.0	mA
T _{STG}	Storage Temperature	-65 to +150	°C

Notes:

- Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Device should not be operated outside the Recommended Operating Conditions.
- The I/O source sink numbers refer to tri-stated inputs and outputs.

9.2. RECOMMENDED OPERATING CONDITIONS

Parameter	Commercial	Industrial	Military	Units
Temperature Range ₁	0 to +70	-40 to +85	-55 to +125	°C
3.3V Power Supply Tolerance	±10	±10	±10	%
5V Power Supply Tolerance	±10	±10	±10	%
2.5V Power Supply Tolerance	±10	±10	±10	%

Note:

- Ambient temperature (TA) is used for commercial and industrial; case temperature (TC) is used for military.

9.3. ELECTRICAL SPECIFICATIONS

Symbol	Parameter	Commercial		Industrial		Units
		Min	Max	Min	Max	
V _{OH}	(I _{OH} = -20uA) (I _{OH} = -8mA)	0.9V _{CCI} 2.4		0.9V _{CCI} 2.4		V
V _{OL}	(I _{OL} = 1mA) (I _{OL} = 12mA)		0.1 V _{CCI} 0.4		0.1 V _{CCI} 0.4	V
V _{IL}	Input Low voltage		0.8		0.8	V
V _{IH}	Input High voltage	2.0		2.0		V
I _{IL}	Input Leakage Current, V _{IN} = V _{CCI} or GND	-10	10	-10	10	µA
I _{OZ}	3-State Output Leakage Current, V _{OUT} = V _{CCI} or GND	-10	10	-10	10	µA
t _R , t _F	Input Transition Time t _R , t _F		10		10	ns
C _{IO}	I/O Capacitance		10		10	pF
I _{CC}	Standby Current		10		20	mA

10. PCI ELECTRICAL COMPLIANCE

PCILite is implemented using an Actel SX-A FPGA, which supports 3.3V and 5V PCI and is compliant with the PCI Local Bus Specification Rev. 2.2.

10.1. DC SPECIFICATIONS (5.0V PCI OPERATION)

Symbol	Parameter	Condition	Min	Max	Units
V _{CCA}	Supply Voltage for Array		2.3	2.7	V
V _{CCI}	Supply Voltage for IOs		4.75	5.25	V
V _{IH}	Input High Voltage ₁		2.0	V _{CCI} + 0.5	V
V _{IL}	Input Low Voltage ₁		-0.5	0.8	V
I _{IH}	Input High Leakage Current	V _{IN} = 2.7		70	μA
I _{IL}	Input Low Leakage Current	V _{IN} = 0.		-70	μA
V _{OH}	Output High Voltage	I _{OUT} = -2 mA	2.4		V
V _{OL}	Output Low Voltage ₂	I _{OUT} = 3 mA, 6 mA		0.55	V
C _{IN}	Input Pin Capacitance		3	10	pF
C _{CLK}	CLK Pin Capacitance		5	12	pF

Notes:

- Input leakage currents include hi-Z output leakage for all bi-directional buffers with tri-state outputs.
- Signals without pull-up resistors must have 3 mA low output current. Signals requiring pull up must have 6 mA; the latter includes, FRAME#, IRDY#, IRDY#, DEVSEL#, STOP#, SERR#, PERR#, LOCK#, and, when used AD[63:32], C/BE[7:4]#, PAR64, REQ64#, and ACK64#.
- Absolute maximum pin capacitance for a PCI input is 10 pF (except for CLK) with an exception granted to motherboard-only devices, which could be up to 16 pF, in order to accommodate PGA packaging. This would mean, in general, that components for expansion boards would need to use alternatives to ceramic PGA packaging (i.e., PQFP, SGA, etc.).

10.2. AC SPECIFICATIONS (5.0V PCI OPERATION)

Symbol	Parameter	Condition	Min	Max	Units
I _{OH(AC)}	Switching ₁ Current High _{1,2} 1,3	0 < V _{OUT} < 1.4	-44	Eq A	mA
		1.4 < V _{OUT} < 2.4	(-44 + (V _{OUT} - 1.4)/0.024)		
	(Test Point) ₃	V _{OUT} = 3.1		-142	mA
I _{OL(AC)}	Switching ₁ Current Low ₁ 1,3	V _{OUT} ³ 2.2	95	Eq. B	mA
		2.2 > V _{OUT} > 0.55	(V _{OUT} / 0.023)		
	(Test Point) ₃	V _{OUT} = 0.71		206	mA
I _{CL}	Low Clamp Current	-5 < V _{IN} < -1	-25 + (V _{IN} + 1)/0.015		mA
slew R	Output Rise Slew Rate ₄	0.4V to 2.4V _{load}	1	5	V/ns
slew F	Output Fall Slew Rate ₄	2.4V to 0.4V _{load}	1	5	V/ns

Notes:

- Refer to the V/I curves that follow. Switching current characteristics for REQ# and GNT# are permitted to be one half of that specified here; i.e., half size output drivers may be used on these signals. This specification does not apply to CLK and RST# which are system outputs. "Switching Current High" specification are not relevant to SERR#, INTA#, INTB#, INTC#, and INTD# which are open drain outputs.
- Note that this segment of the min current curve is drawn from the AC drive point directly to the DC drive point rather than toward the voltage rail (as is done in the pull-down curve). This difference is intended to allow for optional N-channel pull-up.
- Maximum current requirements must be met as drivers pull beyond the last step voltage. Equations defining these maximums (A and B are provided with the respective diagrams below. The equation-defined maxima should be met by design. In order to facilitate component testing, a maximum current test point is defined for each side of the output driver.
- This parameter is to be interpreted as the cumulative edge rate across the specified range, rather than the instantaneous rate at any point within the transition range. The specified load (diagram below) is optional; i.e., the designer may elect to meet this parameter with an unloaded output per revision 2.0 of the PCI Local Bus Specification. However, adherence to both maximum and minimum parameters is now required (the maximum is no longer simply a guideline). Since adherence to the maximum slew rate was not required prior to revision 2.1 of the specification, there may be components in the market for some time that have faster edge rates; therefore, designers must bear in mind that rise and fall times faster than this specification could occur, and should ensure that signal integrity modeling accounts for this. Rise slew rate does not apply to open drain outputs.

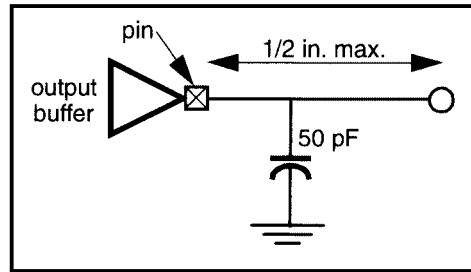


Figure 12. Mechanical specification for connecting PCI pins.

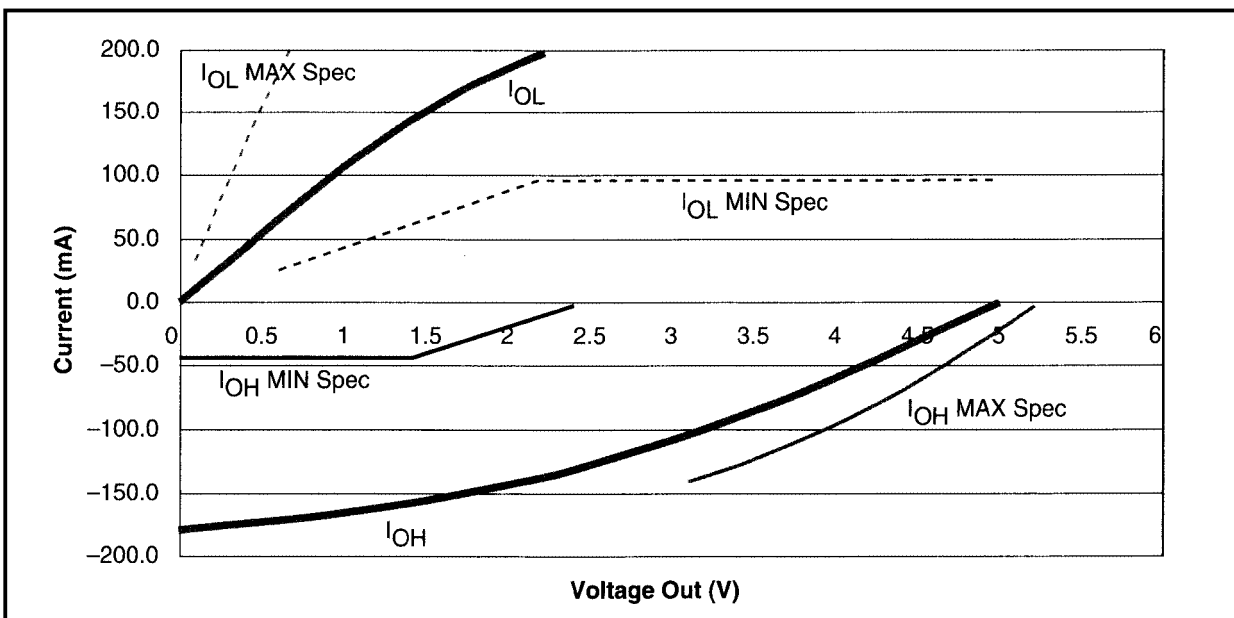


Figure 13. 5.0V PCI V/I curves and the minimum and maximum PCI drive characteristics of the SX-A family.

Equation A:

$$I_{OH} = 11.9 * (V_{OUT} - 5.25) * (V_{OUT} + 2.45)$$

for $V_{CCI} > V_{OUT} > 3.1V$

Equation B:

$$I_{OL} = 78.5 * V_{OUT} * (4.4 - V_{OUT})$$

for $0V < V_{OUT} < 0.71V$

10.3. DC SPECIFICATIONS (3.3V PCI OPERATION)

Symbol	Parameter	Condition	Min	Max	Units
V _{CCA}	Supply Voltage for Array		2.3	2.7	V
V _{CCI}	Supply Voltage for IOs		3.0	3.6	V
V _{IH}	Input High Voltage		0.5V _{CCI}	V _{CCI} + 0.5	V
V _{IL}	Input Low Voltage		-0.5	0.3V _{CCI}	V
V _{ipu}	Input Pull-up Voltage ₁		0.7V _{CCI}		V
I _{IL}	Input Leakage Current ₂	0 < V _{in} < V _{CCI}	-10	+10	μA
V _{OH}	Output High Voltage	I _{OUT} = -500uA	0.9V _{CCI}		V
V _{OL}	Output Low Voltage	I _{OUT} = 1500uA		0.1V _{CCI}	V
C _{IN}	Input Pin Capacitance ₃			10	pF
C _{CLK}	CLK Pin Capacitance		5	12	pF

Notes:

1. This specification should be guaranteed by design. It is the minimum voltage to which pull-up resistors are calculated to pull a floated network. Applications sensitive to static power utilization should assure that the input buffer is conducting minimum current at this input voltage.
2. Input leakage currents include hi-Z output leakage for all bi-directional buffers with tri-state outputs.
3. Absolute maximum pin capacitance for a PCI input is 10 pF (except for CLK)

10.4. AC SPECIFICATIONS (3.3V PCI OPERATION)

Symbol	Parameter	Condition	Min	Max	Units
I _{OH(AC)}	Switching Current High	0 < V _{OUT} ≤ 0.3V _{CCI} ¹ 0.3V _{CCI} ≤ V _{OUT} < 0.9V _{CCI} ¹ 0.7 < V _{OUT} < V _{CCI} ^{1,2}	-12V _{CCI} (-17.1 + (V _{CCI} - V _{OUT}))	Eq. C	mA mA
	(Test Point)	V _{OUT} = 0.7V _{CC} ²		-32V _{CCI}	mA
I _{OL(AC)}	Switching Current Low	V _{CCI} > V _{OUT} > 0.6V _{CCI} ¹ 0.6V _{CCI} > V _{OUT} > 0.1V _{CCI} ¹ 0.18V _{CCI} > V _{OUT} > 0 ^{1,2}	16V _{CCI} (26.7V _{OUT})	Eq. D	mA mA
	(Test Point)	V _{OUT} = 0.18V _{CC} ²		38V _{CCI}	mA
I _{CL}	Low Clamp Current	-3 < V _{IN} < -1	-25 + (V _{IN} + 1)/0.015		mA
I _{CH}	High Clamp Current	V _{CCI} + 4 > V _{in} ≥ V _{CCI} + 1	-25 + (V _{IN} - V _{CCI} - 1)/0.015		
slew R	Output Rise Slew Rate	0.2 V _{CCI} to 0.6 V _{CCI} load ³	1	4	V/ns
slew F	Output Fall Slew Rate	0.6 V _{CCI} to 0.2 V _{CCI} load ³	1	4	V/ns

Notes:

1. Refer to the V/I curves that follow. Switching current characteristics for REQ# and GNT# are permitted to be one half of that specified here; i.e., half size output drivers may be used on these signals. This specification does not apply to CLK and RST# which are system outputs. "Switching Current High" specification are not relevant to SERR#, INTA#, INTB#, INTC#, and INTD# which are open drain outputs.
2. Maximum current requirements must be met as drivers pull beyond the last step voltage. Equations defining these maximums (C and D) are provided with the respective diagrams in below. The equation-defined maxima should be met by design. In order to facilitate component testing, a maximum current test point is defined for each side of the output driver.
3. This parameter is to be interpreted as the cumulative edge rate across the specified range, rather than the instantaneous rate at any point within the transition range. The specified load (diagram below) is optional; i.e., the designer may elect to meet this parameter with an unloaded output per the latest revision of the PCI Local Bus Specification. However, adherence to both maximum and minimum parameters is required (the maximum is no longer simply a guideline). Rise slew rate does not apply to open drain outputs

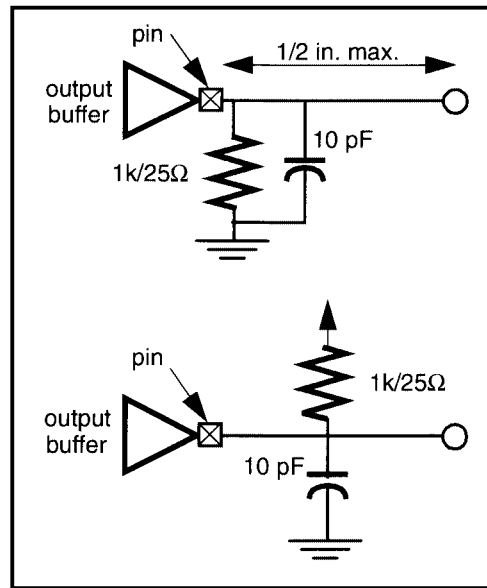


Figure 14. Mechanical specification for connecting PCI pins.

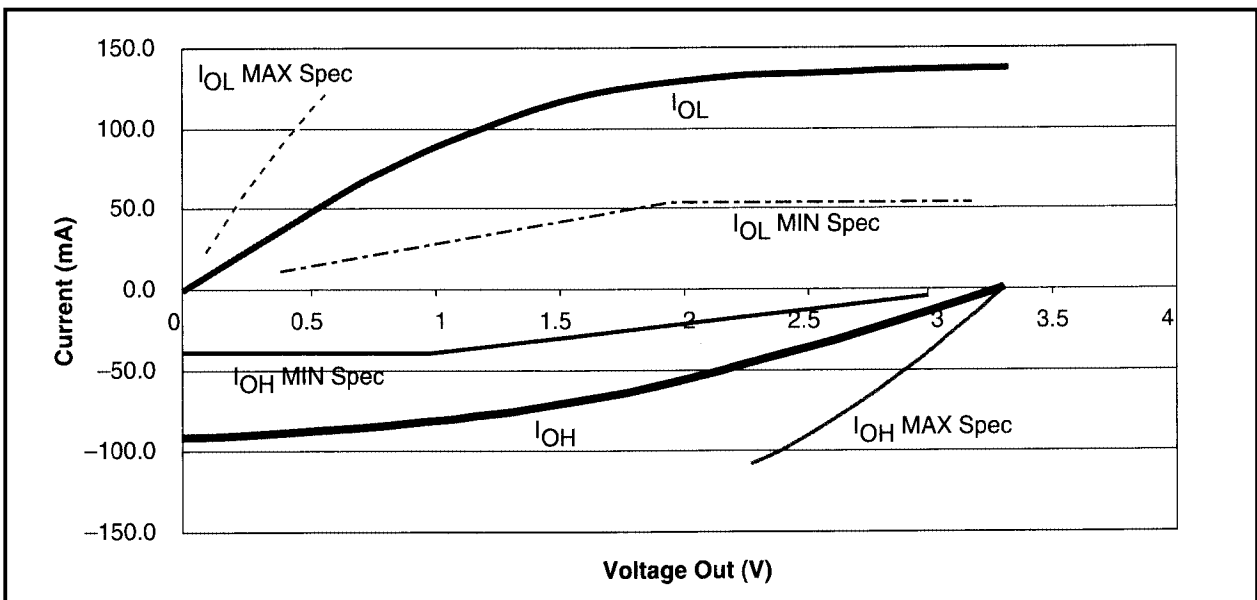


Figure 15. 3.3V PCI V/I curves and the minimum and maximum PCI drive characteristics of the SX-A family.

Equation C:

$$I_{OH} = (98.0/V_{CCI}) * (V_{OUT} - V_{CCI}) * (V_{OUT} + 0.4V_{CCI})$$

for $V_{CCI} > V_{OUT} > 0.7 V_{CCI}$

Equation D:

$$I_{OL} = (256/V_{CCI}) * V_{OUT} * (V_{CCI} - V_{OUT})$$

for $0V < V_{OUT} < 0.18 V_{CCI}$

11. DRIVER INFORMATION

ASIC Design Services provides free PCILite drivers for Windows 98, NT, 2000, Me and XP. The drivers allow the user to communicate with PCILite and write software to work with the device.

The drivers as well as a demo application with source code can be downloaded from www.pcilite.com

12. VENDOR IDs

The following information needs to be supplied to ASIC Design Services for the use of PCILite:

USER_DEVICE_ID
USER_VENDOR_ID
USER_REVISION_ID
USER_BASE_CLASS
USER_SUB_CLASS
USER_PROGRAM_IF
USER_SUBSYSTEM_ID
USER_SUBVENDOR_ID

Refer to PCI specification 2.2 for a full listing on BASE and SUB classes.

Actel has a vendor ID (11AA) that customers are free to use, since PCILite is implemented on an Actel FPGA. Customer's can assign their own vendor ID, or use the Actel ID and then assign their vendor ID in the Sub-vendor ID area.

For a sub vendor ID the user should register with PCISIG to get a sub vendor ID. The user can also register to get a vendor and device ID.

13. EVALUATION BOARD

An evaluation board is available from ASIC Design Services that allows the user to quickly evaluate the operation of PCILite. All the PCILite backend pins are available on headers on the board. This allows the user to easily add their own circuitry and do simple transfers to and from the PCI card using the evaluation software.

In addition, the board has the following memory devices on it:

- 1k-bit Serial EEPROM (64 x 16-bits) - 93LC46B,
- 4 x 128k High speed CMOS static RAM devices – W24010S.

For more information on the PCILite evaluation board, see the “PCILite Evaluation Board Quick Start Guide” which can be obtained from the PCILite website at www.pcilite.com

The schematics for the evaluation board are shown on the following pages. The schematics serve as a good example on how to interface to PCILite.

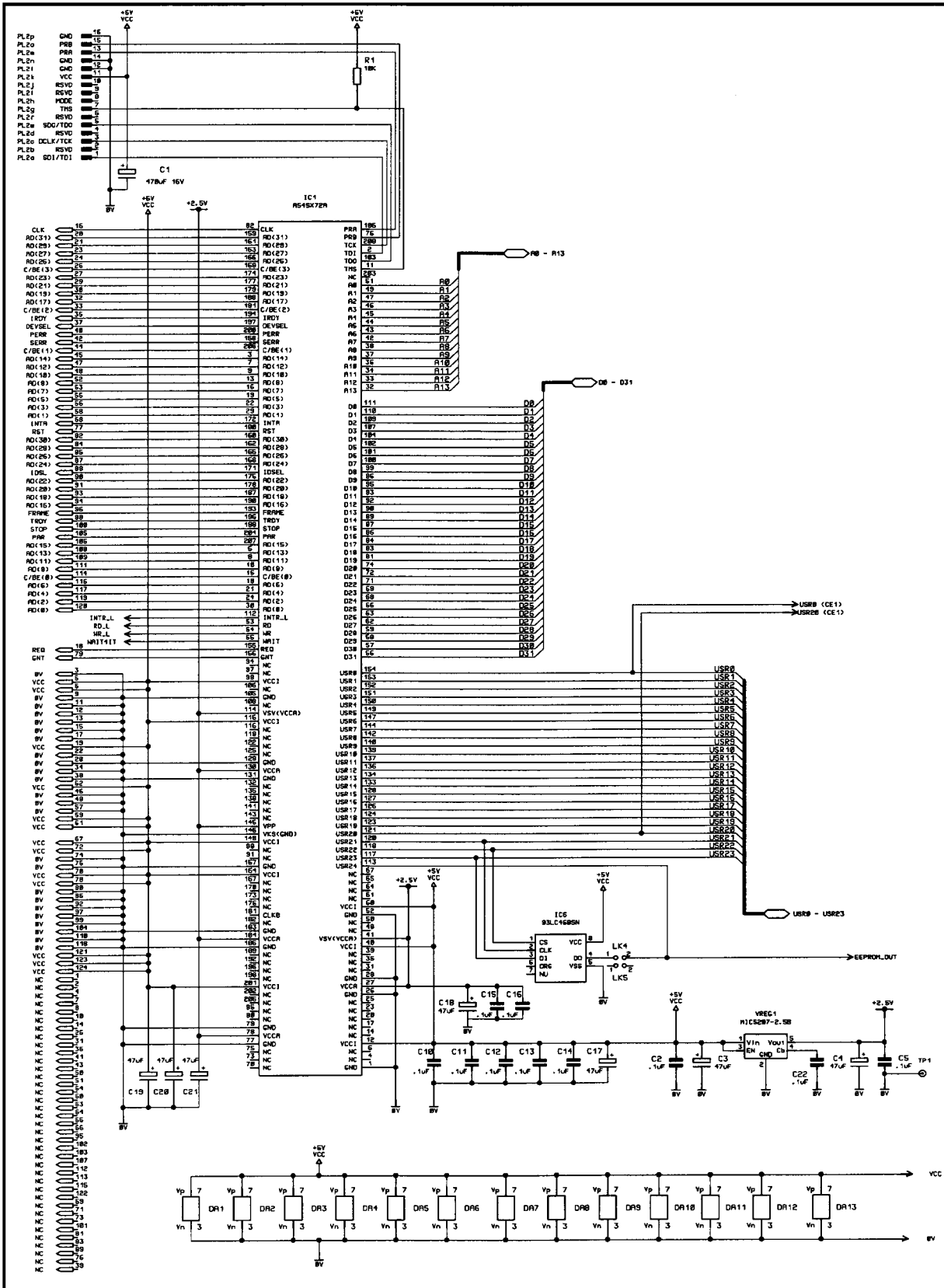


Figure 16. Schematic of PCILite evaluation board.

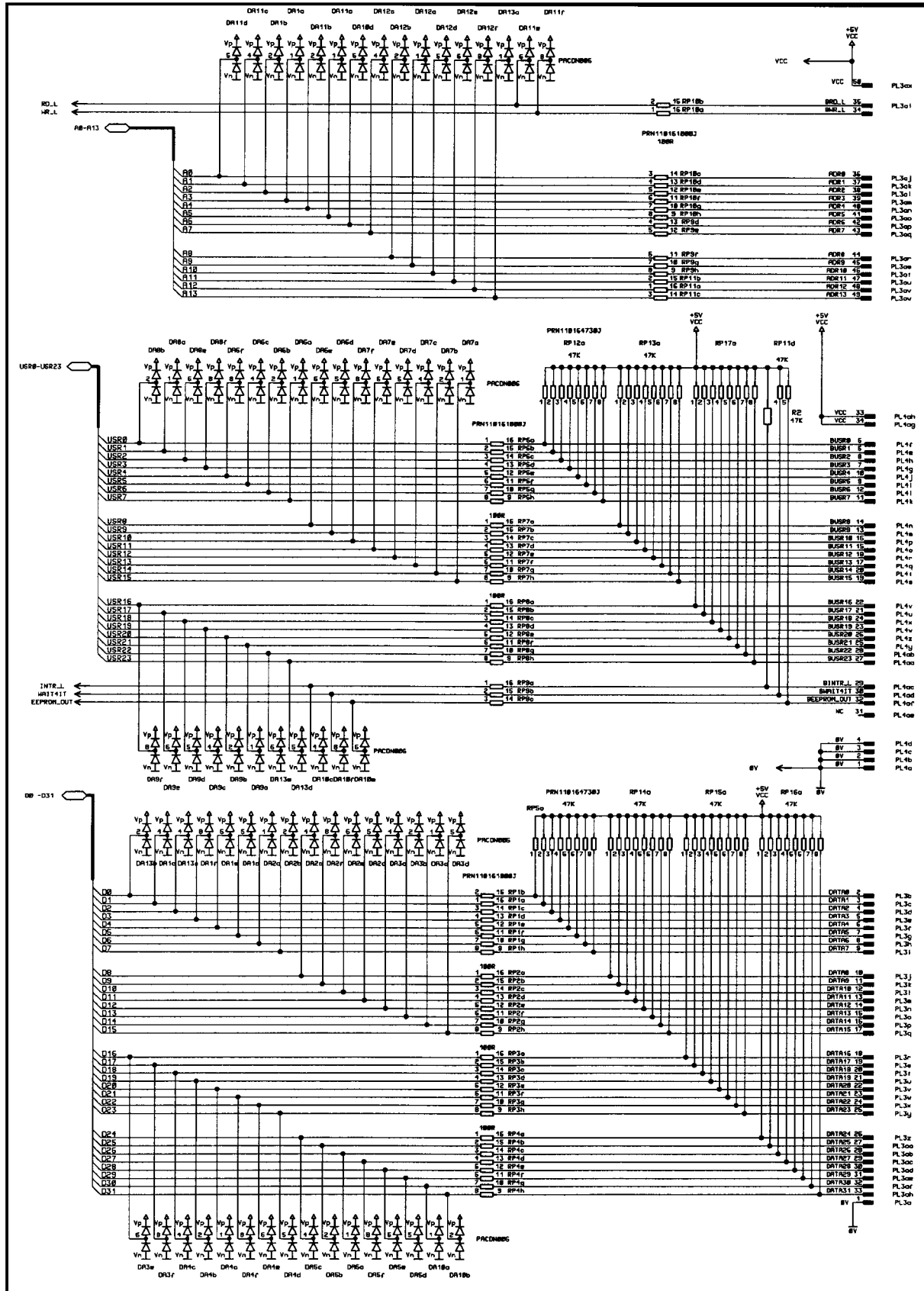
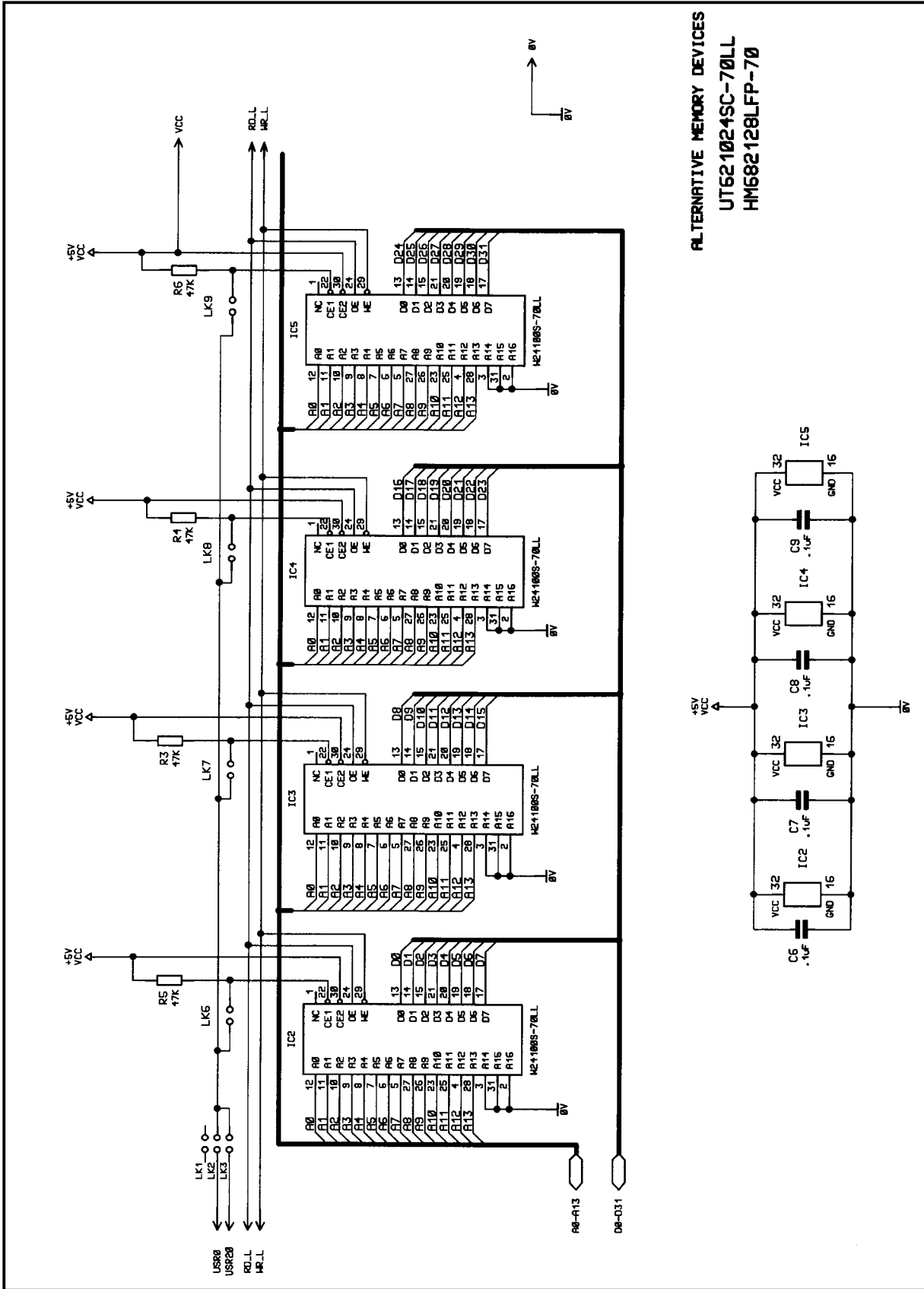


Figure 17. Schematic of PCI Lite evaluation board illustrating the connection of the backend signals.



ALTERNATIVE MEMORY DEVICES
UT621024SC-70LL
HM582128LFP-70

Figure 18. Schematic of PCI Lite evaluation board illustrating interface to memory devices.

14. ORDERING INFORMATION

PART NUMBER	DATABUS WIDTH	PACKAGE
PCILite-8/100	8-bit	TQFP-100
PCILite-16/144	16-bit	TQFP-144
PCILite-32/144	32-bit	TQFP-144
PCILite-32/208	32-bit	PQFP-208

ASIC Design Services cc.
1st Floor West
Thandanani Office Park
Invicta Road
Midrand
South Africa

Tel: +27 +11 315 8316

ASIC Design Services cc.
P.O.Box 5485
Midrand
1685
South Africa

Fax: +27 +11 315 1711

For more information on PCILite contact Kobus van Rooyen at ASIC Design Services:

Tel: +27 11-315 8316 or email info@pcilite.com

Also, see the PCILite website www.pcilite.com and

ASIC Design Services website www.asic.co.za