PCILite Evaluation Board

Quick Start Guide

Version 1.1

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Preface

This Quick Start manual describes the Hardware and Software Installation procedures for the PCILite Evaluation Board.

The Evaluation Board connects the PCILite device to SRAM memory and EEProm devices allowing the user to evaluate the PCILite back-end interface. All user definable IO pins are available on header pins where the user can easily connect additional circuitry.

The PCILite Evaluation Board will assist Design Engineers during initial evaluation and debugging phases of a PCI Design, allowing a short time to market and making PCI easy.

Software drivers are supplied for Windows 95, 98, NT and 2000.

PCILite

PCILite was born out of the requirement for a simple PCI interface.

PCILite is a PCI Target, which allows old ISA card designs to be converted to PCI requiring minimum effort from the designer. PCILite provides an Intel-like microprocessor back-end interface with simple programmable read, write and chip-select signals. PCILite connects to peripherals through a user address and data bus. Additional user pins, definable as inputs, outputs or chip-selects are also provided. PCILite is available in an 8, 16 or 32 bit version.

The smallest package/footprint for PCILite is a standard 100 pin TQFP package with dimensions of only 16mm x 16mm. This saves space on the card for the user's other requirements. Because of the simplicity of PCILite, a PCI application can be developed in a very short space of time.

For customers requiring something more than a PCI Target, PCIPlus is offered. PCI functions such as Master and DMA controller, plus user specific logic functionality, such as glue logic and FIFO interfaces, can be implemented in a single PCIPlus device providing additional logic integration benefits.

Hardware Installation

To install the PCILite Evaluation Board:

1) Switch the computer off and insert the PCILite Evaluation Board in an open PCI slot.

2) Switch on the computer, if Windows PnP (Plug-and-Play) manager is installed and it finds the PCILite Evaluation Board, choose the “Disable Device” which will stop the PnP manager.

3) Browse to :\Install directory on the CD supplied, and execute the PCILite.exe file.

4) Select the appropriate driver to install, as well as the Windows API. Click “next”.
Note: For Windows 2000 there is an option for 2 different drivers, only install 1 of the drivers.

5) Restart your computer when prompted.

Hardware Setup

Jumpers Settings

There are seven jumpers on the PCILite demo board, which are used to connect the four SRAM and one serial EEProm devices.

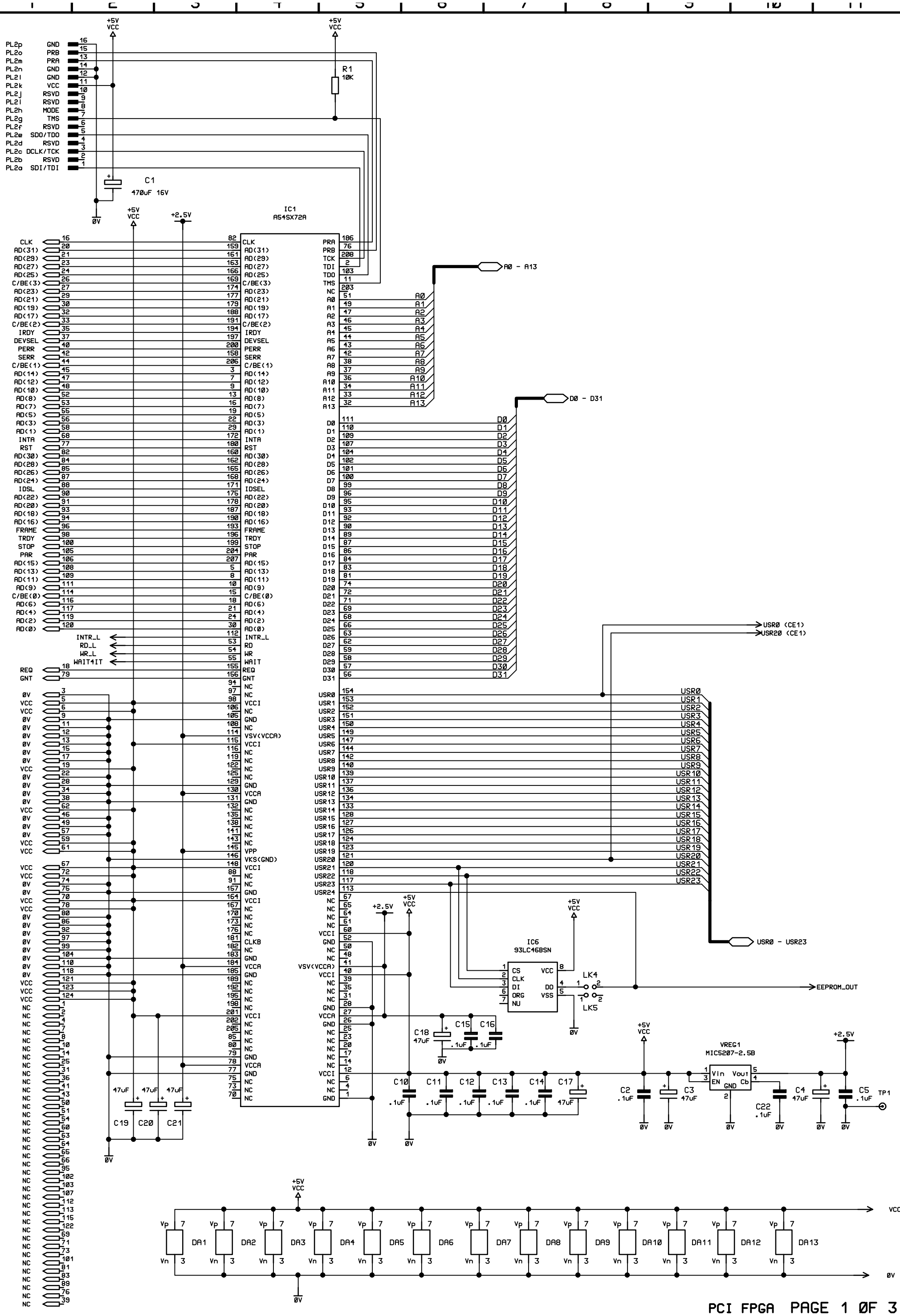
Jumper Connected	Condition
Link 1	Disabled SRAM Devices
Link 2	SRAM chip enable connected to USER pin 0
Link 3	SRAM chip enable connected to USER pin 20
Link 4	EEProm device “data out” pin connected to USER pin 24
Link 5	EEProm device “data out” pin floating
Link 6	SRAM Device 1 enabled
Link 7	SRAM Device 2 enabled
Link 8	SRAM Device 3 enabled
Link 9	SRAM Device 4 enabled

The chip enable pin on the SRAM devices can either be connected to USER pin 0 (Link 2), USER pin 20 (Link 3) or not be connected (Link 1) to any USER pins disabling the SRAM devices.

Links 6, 7, 8, and 9 are used to enable SRAM devices 1, 2, 3 and 4 respectively. When the links are removed, the corresponding SRAM device is disabled.

The "data out" pin of the serial EEProm device is either connected to USER pin 24 (Link 4) or left floating (Link 5).

The use of links further described in the schematics on the following pages.


+5V
VCC
PL2p GND 16
PL2o PRB 15
PL2m PRA 13
PL2n GND 14
PL2l GND 12
PL2k VCC 11
PL2j RSVD 10
PL2i RSVD 9
PL2h MODE 8
PL2g TMS 7
PL2f RSVD 6
PL2e SDO/TDO 5
PL2d RSVD 4
PL2c DCLK/TCK 3
PL2b RSVD 2
PL2a SDI/TDI 1
R1
10K
C1
470uF 16V
0V
IC1
A54SX72A
+2.5V
CLK 16 82
AD(31) 20 159
AD(29) 21 161
AD(27) 23 163
AD(25) 24 166
C/BE(3) 26 169
AD(23) 27 174
AD(21) 29 177
AD(19) 30 179
AD(17) 32 188
C/BE(2) 33 191
IRDY 35 194
DEVSEL 37 197
PERR 40 200
SERR 42 158
C/BE(1) 44 206
AD(14) 45 3
AD(12) 47 7
AD(10) 48 9
AD(8) 52 13
AD(7) 53 16
AD(5) 55 19
AD(3) 56 22
AD(1) 58 29
INTA 68 172
RST 77 180
AD(30) 82 160
AD(28) 84 162
AD(26) 85 165
AD(24) 87 168
IDSL 88 171
AD(22) 90 175
AD(20) 91 178
AD(18) 93 187
AD(16) 94 190
FRAME 96 193
TRDY 98 196
STOP 100 199
PAR 105 201
AD(15) 106 207
AD(13) 108 5
AD(11) 109 8
AD(9) 111 10
C/BE(0) 114 15
AD(6) 116 18
AD(4) 117 21
AD(2) 119 24
AD(0) 120 30
INTR_L 112
RD_L 53
WR_L 54
WAIT4IT 55
REQ 18 155
GNT 79 156
NC 91
NC 97
VCCI 98
NC 106
GND 105
NC 108
VSV(VCCA) 114
VCCI 115
NC 116
NC 119
NC 122
NC 125
NC 129
GND 130
VCCA 131
GND 132
NC 135
NC 138
NC 141
NC 143
NC 145
VPP 146
VKS(GND) 148
VCCI 88
NC 91
NC 157
GND 164
VCCI 167
NC 170
NC 173
NC 176
NC 181
CLKB 182
NC 183
GND 184
VCCA 185
GND 189
NC 192
NC 195
NC 198
NC 201
VCCI 202
NC 205
NC 85
NC 80
NC 79
GND 78
VCCA 77
GND 75
NC 73
NC 70
PRA 186
PRB 76
TCK 208
TDI 2
TDO 103
TMS 11
NC 203
A0 51
A1 49
A2 47
A3 46
A4 45
A5 44
A6 43
A7 42
A8 38
A9 37
A10 36
A11 34
A12 33
A13 32
A0 - A13
D0 111
D1 110
D2 109
D3 107
D4 104
D5 102
D6 101
D7 100
D8 99
D9 96
D10 95
D11 93
D12 92
D13 90
D14 89
D15 87
D16 86
D17 84
D18 83
D19 81
D20 74
D21 72
D22 71
D23 69
D24 68
D25 66
D26 63
D27 62
D28 59
D29 58
D30 57
D31 56
D0 - D31
USR0 154
USR1 153
USR2 152
USR3 151
USR4 150
USR5 149
USR6 147
USR7 144
USR8 142
USR9 140
USR10 139
USR11 137
USR12 136
USR13 134
USR14 133
USR15 128
USR16 127
USR17 126
USR18 124
USR19 123
USR20 121
USR21 120
USR22 118
USR23 117
USR24 113
USR0 (CE1)
USR20 (CE1)
USR0 - USR23
NC 67
NC 65
NC 64
NC 61
NC 60
VCCI 52
GND 50
NC 48
NC 41
VSV(VCCA) 40
VCCI 39
NC 35
NC 31
NC 28
GND 27
VCCA 26
GND 25
NC 23
NC 20
NC 17
NC 14
VCCI 12
NC 6
NC 4
GND 1
IC6
93LC46BSN
CS
CLK
DI
ORG
NU
VCC
DO
VSS
LK4
LK5
EEPROM_OUT
C18 47uF
C15 .1uF
C16 .1uF
C10 .1uF
C11 .1uF
C12 .1uF
C13 .1uF
C14 .1uF
C17 47uF
C19 47uF
C20 47uF
C21 47uF
VREG1
MIC5207-2.5B
Vin
EN
Vout
Cb
GND
C2 .1uF
C3 47uF
C22 .1uF
C4 47uF
C5 .1uF
TP1
DA1
DA2
DA3
DA4
DA5
DA6
DA7
DA8
DA9
DA10
DA11
DA12
DA13
Vp
Vn
PCI FPGA PAGE 1 0F 3

DA11c DA1a DA11a DA12c DA12a DA12e DA13a DA11f

DA11d DA1b DA11b DA10d DA12b DA12d DA12f DA11e

PACDN006

+5V VCC

VCC

VCC 50 PL3ax

RD_L
WR_L

2 15 RP10b
1 16 RP10a

BRD_L 35 PL3ai
BWR_L 34

A0-A13

PRN11016100ØJ
100R

A0 3 14 RP10c ADR0 36 PL3aj
A1 4 13 RP10d ADR1 37 PL3ak
A2 5 12 RP10e ADR2 38 PL3al
A3 6 11 RP10f ADR3 39 PL3am
A4 7 10 RP10g ADR4 40 PL3an
A5 8 9 RP10h ADR5 41 PL3ao
A6 4 13 RP9d ADR6 42 PL3ap
A7 5 12 RP9e ADR7 43 PL3aq

A8 6 11 RP9f ADR8 44 PL3ar
A9 7 10 RP9g ADR9 45 PL3as
A10 8 9 RP9h ADR10 46 PL3at
A11 2 15 RP11b ADR11 47 PL3au
A12 1 16 RP11a ADR12 48 PL3av
A13 3 14 RP11c ADR13 49 PL3aw

DA8a DA8f DA6c DA6a DA6d DA7e DA7c DA7a
DA8b DA8e DA6f DA6b DA6e DA7f DA7d DA7b

PACDN006

USRØ-USR23

PRN11016473ØJ
RP12a RP13a RP17a RP11d
47K

+5V VCC

+5V VCC

R2 47K

VCC 33 PL1ah
VCC 34 PL1ag

PRN11016100ØJ

USRØ 1 16 RP6a BUSRØ 6 PL1f
USR1 2 15 RP6b BUSR1 5 PL1e
USR2 3 14 RP6c BUSR2 8 PL1h
USR3 4 13 RP6d BUSR3 7 PL1g
USR4 5 12 RP6e BUSR4 10 PL1j
USR5 6 11 RP6f BUSR5 9 PL1i
USR6 7 10 RP6g BUSR6 12 PL1l
USR7 8 9 RP6h BUSR7 11 PL1k

100R

USR8 1 16 RP7a BUSR8 14 PL1n
USR9 2 15 RP7b BUSR9 13 PL1m
USR10 3 14 RP7c BUSR10 16 PL1p
USR11 4 13 RP7d BUSR11 15 PL1o
USR12 5 12 RP7e BUSR12 18 PL1r
USR13 6 11 RP7f BUSR13 17 PL1q
USR14 7 10 RP7g BUSR14 20 PL1t
USR15 8 9 RP7h BUSR15 19 PL1s

100R

USR16 1 16 RP8a BUSR16 22 PL1v
USR17 2 15 RP8b BUSR17 21 PL1u
USR18 3 14 RP8c BUSR18 24 PL1x
USR19 4 13 RP8d BUSR19 23 PL1w
USR20 5 12 RP8e BUSR20 26 PL1z
USR21 6 11 RP8f BUSR21 25 PL1y
USR22 7 10 RP8g BUSR22 28 PL1ab
USR23 8 9 RP8h BUSR23 27 PL1aa

INTR_L
WAIT1IT
EEPROM_OUT

1 16 RP9a
2 15 RP9b
3 14 RP9c

BINTR_L 29 PL1ac
BWAIT1IT 30 PL1ad
BEEPROM_OUT 32 PL1af
NC 31 PL1ae

PACDN006

DA9f DA9d DA9b DA13e DA10c DA10f DA10e
DA9e DA9c DA9a DA13d

ØV 4 PL1d
ØV 3 PL1c
ØV 2 PL1b
ØV 1 PL1a

ØV

DØ -D31

PRN11016473ØJ
RP5a RP14a RP15a RP16a
47K

+5V VCC

ØV

PACDN006

DA13b DA1c DA13c DA1f DA1e DA1d DA2a DA2b DA2c DA2f DA2e DA2d DA3c DA3b DA3a DA3d

PRN11016100ØJ

DØ 2 15 RP1b DATAØ 2 PL3b
D1 1 16 RP1a DATA1 3 PL3c
D2 3 14 RP1c DATA2 4 PL3d
D3 4 13 RP1d DATA3 5 PL3e
D4 5 12 RP1e DATA4 6 PL3f
D5 6 11 RP1f DATA5 7 PL3g
D6 7 10 RP1g DATA6 8 PL3h
D7 8 9 RP1h DATA7 9 PL3i

100R

D8 1 16 RP2a DATA8 10 PL3j
D9 2 15 RP2b DATA9 11 PL3k
D10 3 14 RP2c DATA10 12 PL3l
D11 4 13 RP2d DATA11 13 PL3m
D12 5 12 RP2e DATA12 14 PL3n
D13 6 11 RP2f DATA13 15 PL3o
D14 7 10 RP2g DATA14 16 PL3p
D15 8 9 RP2h DATA15 17 PL3q

100R

D16 1 16 RP3a DATA16 18 PL3r
D17 2 15 RP3b DATA17 19 PL3s
D18 3 14 RP3c DATA18 20 PL3t
D19 4 13 RP3d DATA19 21 PL3u
D20 5 12 RP3e DATA20 22 PL3v
D21 6 11 RP3f DATA21 23 PL3w
D22 7 10 RP3g DATA22 24 PL3x
D23 8 9 RP3h DATA23 25 PL3y

100R

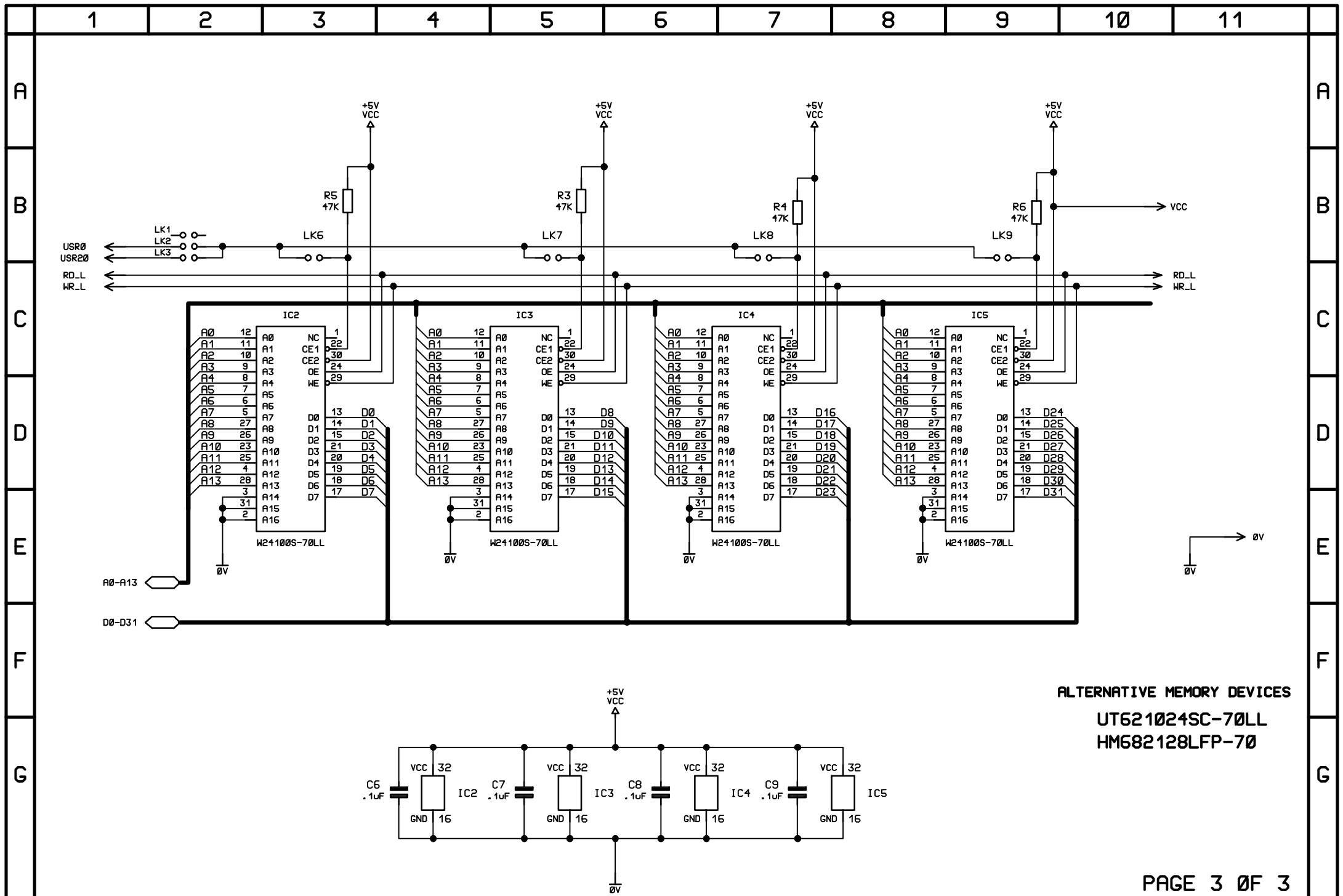
D24 1 16 RP4a DATA24 26 PL3z
D25 2 15 RP4b DATA25 27 PL3aa
D26 3 14 RP4c DATA26 28 PL3ab
D27 4 13 RP4d DATA27 29 PL3ac
D28 5 12 RP4e DATA28 30 PL3ad
D29 6 11 RP4f DATA29 31 PL3ae
D30 7 10 RP4g DATA30 32 PL3af
D31 8 9 RP4h DATA31 33 PL3ah
ØV 1 PL3a

ØV

DA3e DA4c DA4a DA4e DA5c DA5a DA5e DA10a
DA3f DA4b DA4f DA4d DA5b DA5f DA5d DA10b

PACDN006

DATA INTERFACE PAGE 2 ØF 3



ALTERNATIVE MEMORY DEVICES

UT621024SC-70LL
HM682128LFP-70

Header Pinouts

Connector 1

1	GND	2	D0
3	D1	4	D2
5	D3	6	D4
7	D5	8	D6
9	D7	10	D8
11	D9	12	D10
13	D11	14	D12
15	D13	16	D14
17	D15	18	D16
19	D17	20	D18
21	D19	22	D20
23	D21	24	D22
25	D23	26	D24
27	D25	28	D26
29	D27	30	D28
31	D29	32	D30
33	D31	34	WR_L
35	RD_L	36	A0
37	A1	38	A2
39	A3	40	A4
41	A5	42	A6
43	A7	44	A8
45	A9	46	A10
47	A11	48	A12
49	A13	50	VCC

Connector 2

1	GND	2	GND
3	GND	4	GND
5	USR1	6	USR0
7	USR3	8	USR2
9	USR5	10	USR4
11	USR7	12	USR6
13	USR9	14	USR8
15	USR11	16	USR10
17	USR13	18	USR12
19	USR15	20	USR14
21	USR17	22	USR16
23	USR19	24	USR18
25	USR21	26	USR20
27	USR23	28	USR22
29	INTR_L	30	WAIT4IT
31	N/C	32	EEProm_IN
33	VCC	34	VCC

Note: Pin 1 on the header connectors is indicated with a triangle on the side of the connector.

Software Installation

To install the PCILite Demo Software:

1) Create a directory on your hard disk to store the PCILite software in.

2) Copy the file demo.exe from the folder :\Demo to the directory just created.

3) Run the demo.exe file to start the program.

Using the PCILite Demo software

The PCILite Demo Software allows the user to:

1) Set up the USER Pins
2) Set up the Configuration Register
3) Write to the SRAM Memory Devices
4) Read from the SRAM Memory Devices
5) Read the USER Pins

1) Setting up the USER Pins

USER Pins 0 to 20 can be configured as inputs, outputs or chip-select outputs. PCILite registers REG0 and REG1 are used to configure the USER Pins. The registers are 21 bits wide with the first bit (left most bit) representing USER Pin 20. It then follows that bit 21 (right most bit) represents USER Pin 0.

Table 1 below shows how user pin N can be configured using REG0 and REG1.

REG1[N]	REG0[N]	USR[N] function
0	0	Input
0	1	Active low output
1	0	Active low chip-select output
1	1	Active high output

Table 1. User pin configuration

To configure the USER Pins a conversion is required from the binary register value to a decimal value, which is then entered into the PCILite Demo Software.

An example follows.

Example 1:

To configure the USER Pins with pins 0 – 4 as inputs, pins 5 – 9 as active low outputs, pins 10 – 14 as active low chip-select outputs and pins 15 – 20 as active high outputs, the conversion is as follows.

REG0 and REG1 must be set up as:

	20	**19**	**18**	**17**	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
REG1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
REG0	1	1	1	1	1	1	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0

The conversion to decimal:

REG1 = 11111111110000000000 converts to
REG1 = 2096128
REG0 = 11111000001111100000 converts to
REG0 = 2065376

These decimal values are used in the PCILite Demo Software to configure the USER Pins.

2) Setting up the Configuration Register

The configuration register allows setting up the following parameters for PCILite:

Setup: Specifies how many clock cycles the DATA and ADDRESS lines must be stable for before the WR_L signal will go low. The number of cycles is equal to the entered value plus 1. This is a 3-bit value; thus a maximum of 8 clock cycles can be selected.

Duration: Specifies the width (number of clock cycles) of the WR_L or RD_L pulse. The amount of cycles is equal to the entered value plus 1. This is a 3-bit value; thus a maximum of 8 clock cycles can be selected.

Hold: Specifies how many clock cycles the DATA and ADDRESS lines must be kept stable after WR_L or RD_L go high. The amount of cycles is equal to the entered value. This is a 3-bit value; thus a maximum of 7 clock cycles can be selected.

Hold_mode: This is a single bit which places PCILite in the hold_mode causing the RD/WR cycle to be stopped just after the RD_L or WR_L signal has gone low. See the PCILite datasheet for more information. **Warning:** Do not enable this mode unless the WAIT4IT pin is connected to the appropriate circuitry.

EEProm_EN: This is a single bit which when high allows the EEProm interface to use USER pins 21 to 24. When the bit is low, USER pins 21 to 24 will function as USER input pins.

In the Configuration Register, the Setup value occupies bits [2:0], the Duration value occupies bits [6:4], the Hold value occupies bits [10:8], the Hold_mode bit is bit 12 and the EEProm_EN bit is bit 14. Bits 3, 5, 7, 11 and 13 are not used and should be set to 0. Bit 15 is a read-only bit that is high whenever the EEProm is transmitting or receiving data and cannot be set by the user.

The Configuration register is defined as:

BIT	15	14	13	12	11	[10:8]	7	[6:4]	3	[2:0]
USE	EEProm_busy	EEProm_en	n/u	Hold_mode	n/u	Hold	n/u	Duration	n/u	Setup

To configure the Configuration Register a conversion is required from the binary register value to a decimal value, which is then entered into the PCILite Demo Software.

An example follows.

Example 2:

To set the configuration register so that the Setup time is 5 clock cycles, the Duration is 3 clock cycles, the Hold time is 6 clock cycles, Hold mode is not enabled and the EEProm interface is enabled, the conversion is as follows.

The configuration register must be set as:

BIT	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	0	1	0	0	0	1	1	0	0	0	1	0	0	1	0	0

When converted to decimal the value is:

1111111110000000000 converts to 17700

Enter this decimal value in the “configuration” field and click the “configure” button.

3) Writing to the memory devices

The PCILite Demo Board has 4 x SRAM (128 KB each) devices, to which the user can read or write data. These memory devices can only be used if enabled by placing the jumpers in correct places and enabling either USER pin 0 or 20 (depending on where the jumper is) as a chip-select. For example to write one double word (32 bits) to a memory location when using USER pin 0 as a chip-select:

Enable all the SRAM devices by placing jumpers on links 6 to 9. Place a jumper on link 2 (make sure there is no jumper on link 3) to connect the chip enable pins of the SRAM devices to USER pin 0. Configure USER pin 0 as an active low chip-select output using the procedure shown in example 1.

Choose a memory location to where you want to write the data and enter the decimal value of the location in the "offset" field.

Note: Because PCILite uses double word transfers, only every 4^{th} address can be written to, i.e. valid addresses are 0, 4, 8, 12, 16, 20… etc.

Enter the decimal value of the data that is to be stored in the memory in the "value" field.
Click the "write" button.

Example 3:
To store the value A09F1B4xh in memory location 2Cxh, the procedure is as follows:

- The decimal conversion of 2Cxh is 44. Enter this value in the "offset" field.
- The decimal conversion of A09F1B4xh is 168423860. Enter this value in the "value" field.
- Click the "write" button to store the data in the memory location.

4) Reading from the memory devices

To read a value that is stored in a specific location in the on-board memory:

Enter the decimal value of the memory address that is to be read in the "offset" field.
Click the "read" button.
The data stored in the specified memory location will be displayed in the "value" field.

Example 4:
To read back the value that was stored in location 2Cxh in example 3:

- The decimal conversion of 2Cxh is 44. Enter this value in the “offset” field.
- Click the “read” button and the value 168423860 should appear in the “value” field.

5) Reading the user pins

The PCILite Demo Board has the 24 USER Pins connected to the header on the top of the board (the pinouts of the header can be found in the Hardware Setup section). If these pins are configured as inputs (see how in example 1) the values being placed on the pins can be read using the demo software. To do this:

Simply click the “read user” button and the value on the user pins will be displayed in the “user input” field.

Note: If some of the user pins are configured as outputs, then when they are read, the values being written to the pins by PCILite will be returned in the “user input” field.